Midterm Bench Exam

ECE 554

Digital Engineering Laboratory

Nam Sung Kim

(Chunhua Yao –TA)

Exam Schedule

- February 26 (Thursday)
- In Lab
- Duration – Approximately one hour

Background Needed

- Knowledge of logic and digital system design
- Knowledge of Verilog design and debugging
- Knowledge of Modelsim Verilog simulation
- Knowledge of the Xilinx tools and their use
- Knowledge of the FPGA board and its use

Bench Exam Overview

- You will be given a specification for a small system along with Verilog code for some pre-designed modules for the system.
- You will be expected to:
  - Understand the specification
  - Understand the Verilog code provided
  - Write one or more Verilog modules
  - Debug one or more Verilog modules
  - Simulate one or more modules and the entire system
  - Synthesize and implement the design
  - Download, test, and demonstrate the design on the FPGA board

Things to keep in mind

- The bench exam is open book, but no electronic media may be used
  - You may not access any personal or team files
- Each person will take the exam individually
  - Assigned a workstation and FPGA board
- You will have roughly 1 hour to complete the midterm
  - Sign up sheets will be available in the lab
- Successful implementation and demonstration of the design (roughly 70% of grade) is more important than finding and correcting all the errors (roughly 30% of grade).

Rough Outline of Exam

- You will be provided a copy of directions for the exam and system specification – read these over before starting
- You will be provided a copy of necessary files in the “E:\Work\” directory and a read-only copy in the “E:\554 Read Only\” directory
  - Use E:\554 Read Only if you want to “start over”
- You will be given a module with possible bugs (syntax, synthesis, implementation) that you will be asked to fix – You may print, compile, etc. to debug and fix the module
- You will need to find 3-4 errors in the design. For each error you MAY need to
  - Identify symptom of error or mark it on the simulation trace
  - Locate the cause of the error (give module name and line number)
  - Correct the error – print a copy of correct code and highlight your changes
- You may be asked to functionally simulate your design in Modelsim – force files will be provided – print the traces
- You will be given a module with functional description that you will need to write in verilog and integrate it with the remaining design

Rough Outline of Exam

- Synthesize the design - be sure to include all the *.v files
- Implement the design
  - Print a copy of the first page of the map report and the entire post-layout timing report
  - Answer questions related to the reports
- Simulate the timing behavior of your design – force files will be provided – print a copy of your simulation output
- Load the design onto the board
  - If it doesn't work according to the specification, perform further debugging
  - Demonstrate your design to the TA and have the TA sign off on your exam