ECE 4514: Digital Design II – Spring 2008 – CRN 11953

General

- Class Section Meeting Times
  - CRN 11953, Tuesday and Thursday 11:00AM-12:15PM, Durham 261
- Instructor
  - Prof. P. Schaumont
    Durham Hall 361
    540-231-3553
    E-mail: schaum@vt.edu
    WWW: http://www.ece.vt.edu/schaum
- TA:
  - Sandesh Prabhakar
    E-mail: sandeshp@vt.edu
- Office Hours:
  - Schaumont - Tuesday, 4:00PM – 5:00PM,
  - Schaumont - Friday, 11:00AM – 12:00PM,
  - Prabhakar - Thursday 6:00PM – 10:00PM (in the CEL)
- Class Webpage: http://learn.vt.edu

Objectives

In this course, students will learn to use a hardware description language (Verilog) in the digital design process. Emphasis will be on system level concepts and high-level design representations. Methods will be learned that are appropriate for use in automated synthesis systems. Students will have the opportunity to use a commercial computer aided engineering (CAE) tool to design a series of increasingly complex devices. Students will also have the opportunity to use a commercial synthesis tool to automatically map high-level descriptions to Field Programmable Gate Arrays (FPGAs).

Prerequisites

All material in ECE 3504 is important. Specifically, familiarity with Boolean Algebra, logic gates, flip flops, registers, counters, ROMs, PLAs, multiplexers, and sequential circuits in Moore and Mealy form will be assumed. A grade of C- or better in ECE 3504 is required in order for you to enroll in ECE 4514 (enforced by the department).

Required Materials and Textbook

- You will have to purchase a Spartan 3E starter kit ($109), for use in the system design project in this course. The Spartan 3E starter kit is the same one that is used in other computer engineering courses of the department. Special arrangements were made for Virginia Tech regarding the ordering procedure and access to the related design software. Follow the instructions on Blackboard regarding this procedure.
- You also need a DVD with design software for the Spartan 3E starter kit. In spring 2008, the tool versions have been upgraded to ISE 9.2. While the course assignments will not specifically rely on specific features of ISE 9.2, it is

recommended that you upgrade to the latest version of the tools. You will need activation codes to install the software on the DVD. The activation codes will be distributed in class *only*. They will not be communicated in any other way. You will also need additional design software which will be downloaded through the Internet. Please refer to Blackboard for specific instructions.

- The textbook for this course is "*Verilog HDL: A Guide to Digital Design and Synthesis (Second Edition)*", by S. Palnitkar. Additional materials and weblinks will be posted on Blackboard.

Assignments

- There will be **5 homeworks** over the semester, and there will be **5 projects**.
    - Each assignment must be solved in one (or, exceptionally, two) weeks. The exact turn-in date for each assignment will be provided with the assignment.
    - Assignments will be posted on Blackboard and advertised in class, through email, and on the Blackboard Announcements area.
    - There is no late policy in this course. Turning in late assignments is not possible. Homework assignments on paper will be turned at the start of the lecture on the due date. Some assignments will be turned in electronically using Blackboard. The timestamp of Blackboard counts as the turn-in time.
    - You are responsible to keep your class equipment in good working order. Your Spartan kit, your laptop computer, your design files, your design software, all have to be kept in good working condition. Late assignments because of technical issues are not accepted.
- Unless explicitly stated otherwise, all assignments are individual assignments and must be completed by yourself. You can use the Discussion Board on Blackboard to discuss the assignments within the limits of the Honor Code Policy provided below.

GTA Availability

Graduate student assistance will be available in the CEL (368 Durham). The schedule will be posted on the CEL website and announced at the entrance of the CEL. One or more assistants will be designated as ECE4514 assistants. Due to the technical nature of the ECE4514 material, it is unlikely that other graduate assistants will be able to help you. Please try to get GTA assistance first. If that attempt fails, see your instructor during office hours.

Grading

Semester grades will be based on the following weights.

- Homework Assignments (5 in total): 15% of the points
- Project Assignments (5 in total): 45% of the points
- Midterm : 20% of the points
- Final Examination: 20% of the points

- A midterm or final may be rescheduled exceptionally for an individual student provided a valid reason has been approved by the instructor at least one week before the exam date.
- If you feel that an error was made in the grading of your assignment, please present a written appeal to the instructor within one week after the assignment was returned to you. Verbal appeals are not allowed, and grades will not be changed after the one-week period.

Honor Code Policy

Adherence to the Virginia Tech Honor Code is expected in all phases of this course. Any work that you submit for a grade must be your own. Violations will be reported to the Office of the Honor System.

- You may discuss general concepts with your colleagues. It is a violation of the honor code to discuss project solutions or exercise solutions.
- Unless given as a team project, all assignments are individual projects and must contain your own work. All external source code material used must be properly cited. It is a violation of the honor code to provide others access to your solution source code. It is also a violation to access other students' solution files.
- Midterm and Final are individual.
- See http://www.honorsystem.vt.edu for information about Virginia Tech's Undegraduate Honor System and http://www.gradhonor.grads.vt.edu for information about the Graduate Honor System.

Special Needs

- Reasonable accommodations are available for students who have documentation of a disability from a qualified professional. Students should work through Services for Students with Disabilities (SSD) in 152 Henderson Hall. Any student with accommodations through the SSD Office should contact the instructor during the first two weeks of the semester.
- If participation in some part of this class conflicts with your observation of specific religious holidays during the semester, please contact the instructor during the first two weeks of class to make alternative arrangements.
- If you miss class due to illness, especially in the case of an exam or some deadline, see a professional in Schiffert Health Center. If deemed appropriate, documentation of your illness will be sent to the Dean's Office for distribution to the instruction.
- If you experience a personal or family emergency that necessitates missing class, contact the Dean of Students at 231-3787 or see them in 152 Henderson Hall.

Tentative Schedule

Wk	Date	Lec	Topic	HW
1	15-Jan-08	L1	Introduction and Overview	HW1
	17-Jan-08	L2	(L) Hierarchical Modeling	
2	22-Jan-08	L3	(L) Modeling Elements in Verilog	HW2
	24-Jan-08	L4	(L) Gate-level Modeling	
3	29-Jan-08	L5	(T) HDL Simulators	HW3
	31-Jan-08	L6	(D) Design and Simulation of an RNG	
4	05-Feb-08	L7	(L) Dataflow Modeling	HW4
	07-Feb-08	L8	(T) Multiplexed Data-paths	
5	12-Feb-08	L9	(L) System Commands & Testbenches	HW5
	14-Feb-08	L10	(L) Behavioral Modeling 1	
6	19-Feb-08	L11	(D) Design of a SHA-1 hashing module	PJ1
	21-Feb-08	L12	(L) Behavioral Modeling 2	
7	26-Feb-08	R1	Review Lecture	
	28-Feb-08		Midterm	
8	04-Mar-08		No Class (Spring Break)	
	06-Mar-08		No Class (Spring Break)	
9	10-Mar-08	L13	(T) Logic Synthesis	PJ2
	13-Mar-08	L14	(D) FPGA Technology	
10	18-Mar-08		No Class (Instructor on Conference)	PJ3
	20-Mar-08	L15	(D) Control in FPGA	
11	25-Mar-08	L16	(T) Memory and Datapath in FPGA	PJ4
	27-Mar-08	L17	(D) Design of a Reed Solomon Coder	
12	01-Apr-08	L18	(T) Optimizing Area	
	03-Apr-08	L19	(T) Optimizing Speed	
13	08-Apr-08	L20	(D) Timing Analysis and Simulation	PJ5
	10-Apr-08	L21	(L) Tasks and Functions, PLI	
14	15-Apr-08	L22	(T) Testing and Verification	
	17-Apr-08	L23	(D) Design of a RISC Processor	
15	22-Apr-08		Project Discussion/Presentation	
	24-Apr-08		Project Discussion/Presentation	
16	29-Apr-08	R2	Review Lecture	
	05-May-08		Final Exam	

- Lectures codes: (L) Verilog Language, (D) Design Example, (T) Tools and methodology
- Homwework codes indicate hand-out date: HWx Homework, PJx Project