ECE 4514
Digital Design II
Spring 2008

Lecture 14:
The Spartan 3E FPGA

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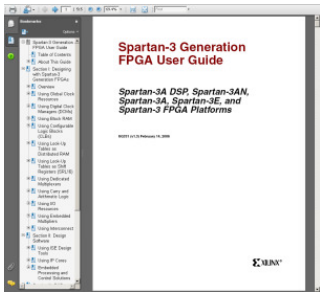
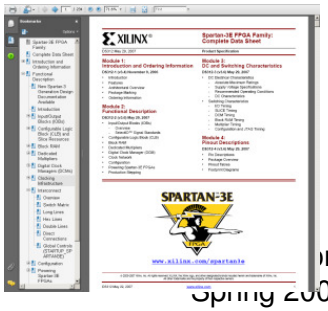
FPGA Internals: The Spartan 3ES500 FPGA

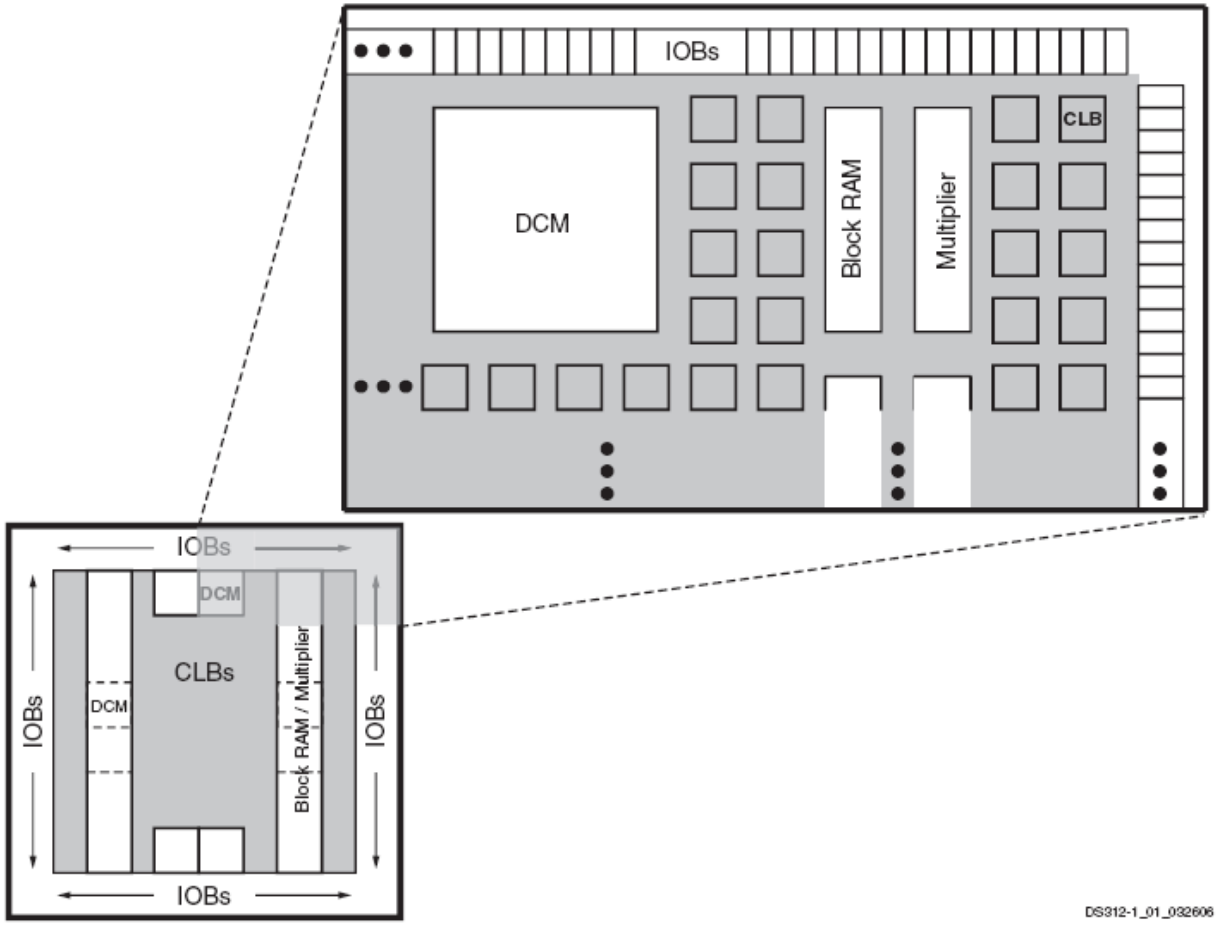
- The internals of an FPGA
  - focus on the Spartan 3ES500 FPGA
- Objectives:
  - Understand how an FPGA can implement arbitrary circuits written in Verilog
  - Identify important metrics of FPGA capacity and features
  - Understand FPGA 'speak' used by design tools: LUT, LC, BRAM, DCM, IOB, ..
- Two important documents for the Spartan 3E FPGA
  - 'Spartan 3E Family Complete Datasheet'
  - 'Spartan 3 User Guide'





Spartan 3

- 5 programmable elements in a regular network



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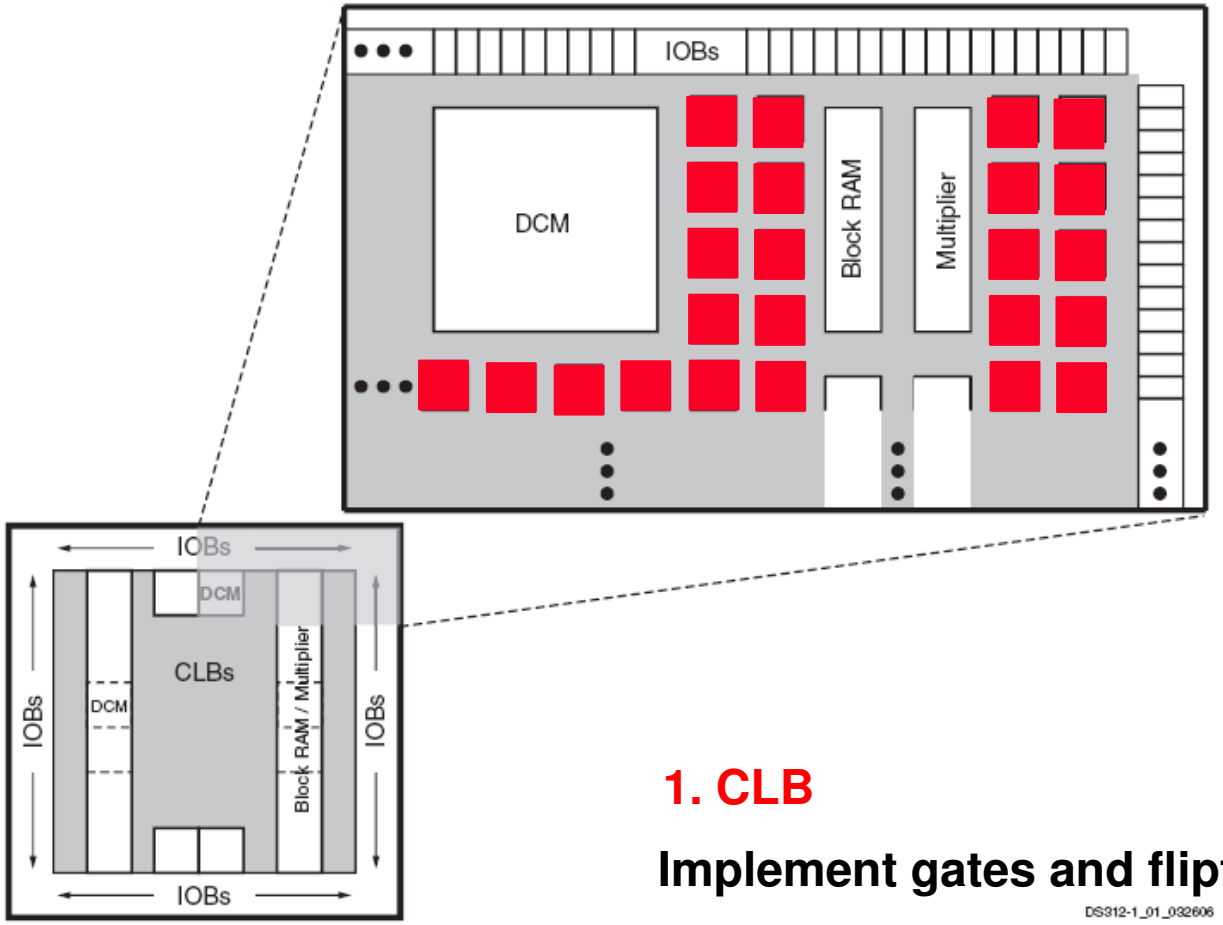

1. CLB

Implement gates and flipflops

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Spartan 3

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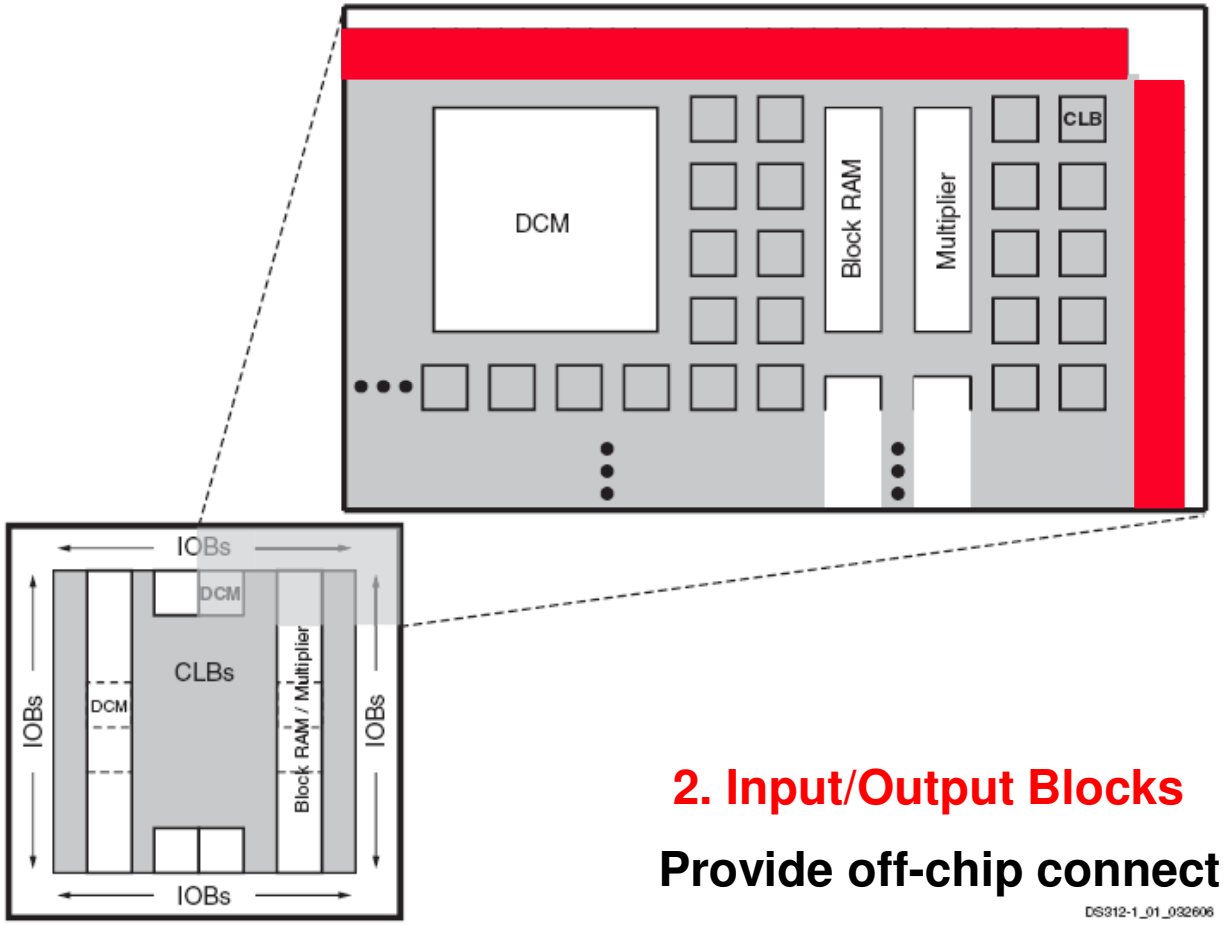

2. Input/Output Blocks

Provide off-chip connectivity

Spartan 3

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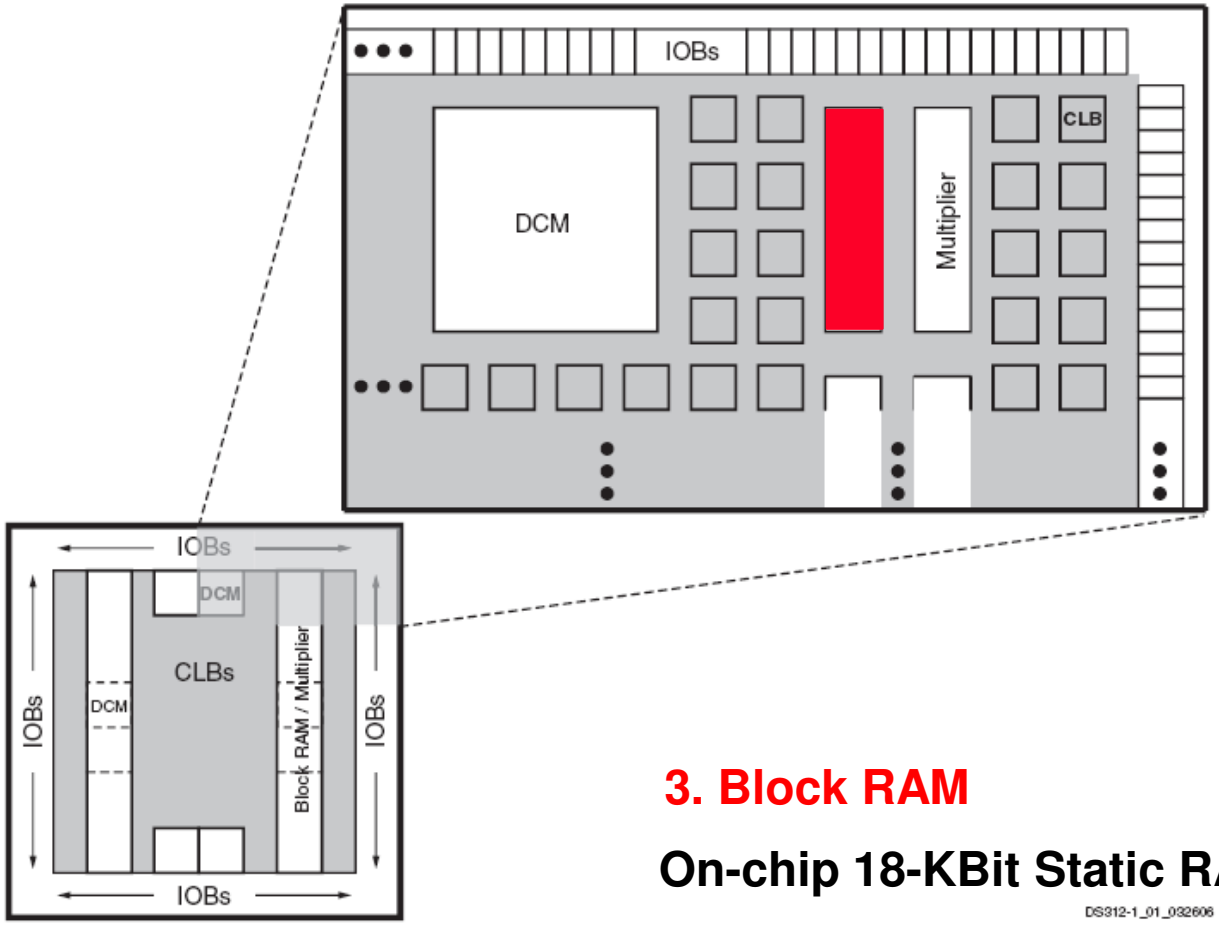

3. Block RAM

On-chip 18-KBit Static RAM storage

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Spartan 3

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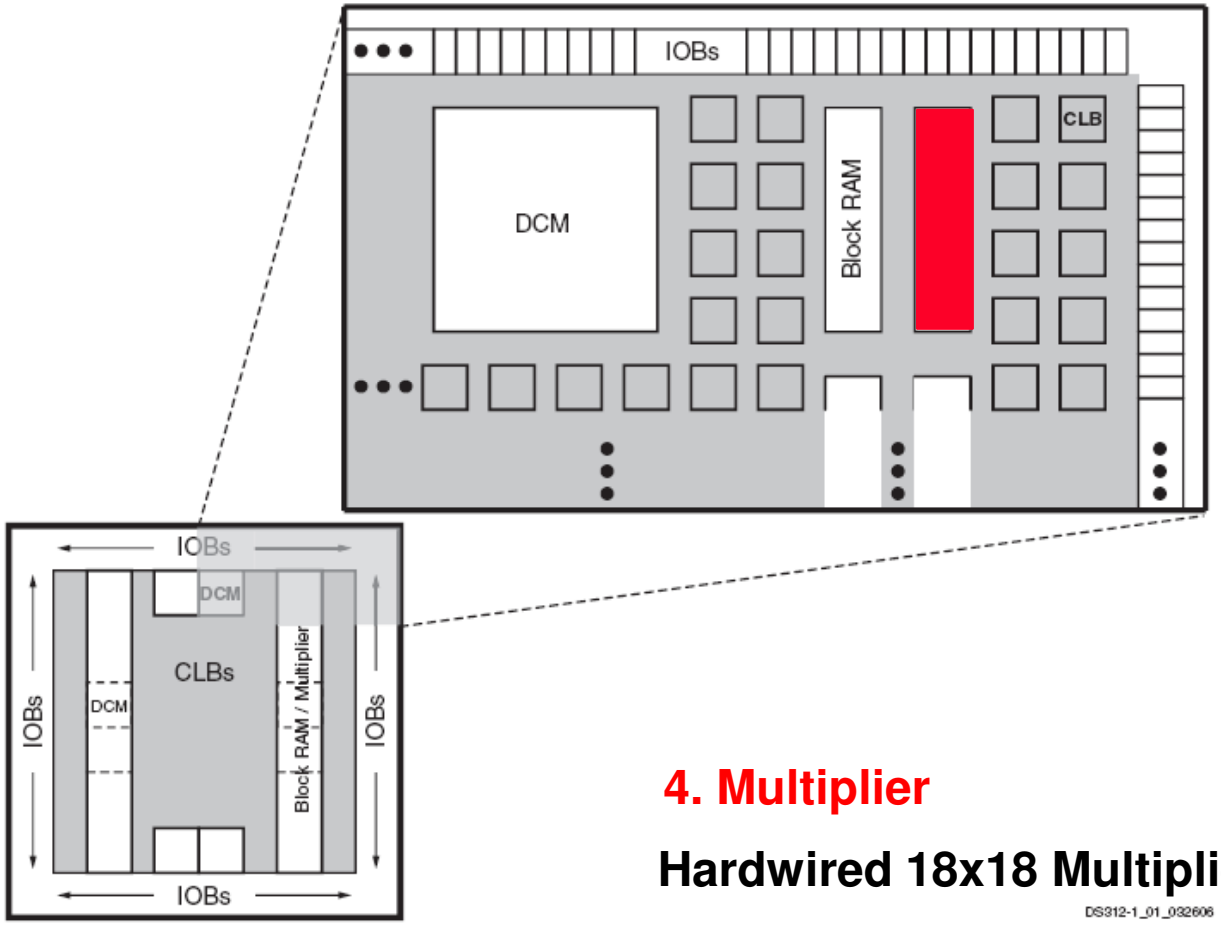

4. Multiplier

Hardwired 18x18 Multiplier Cell

Spartan 3

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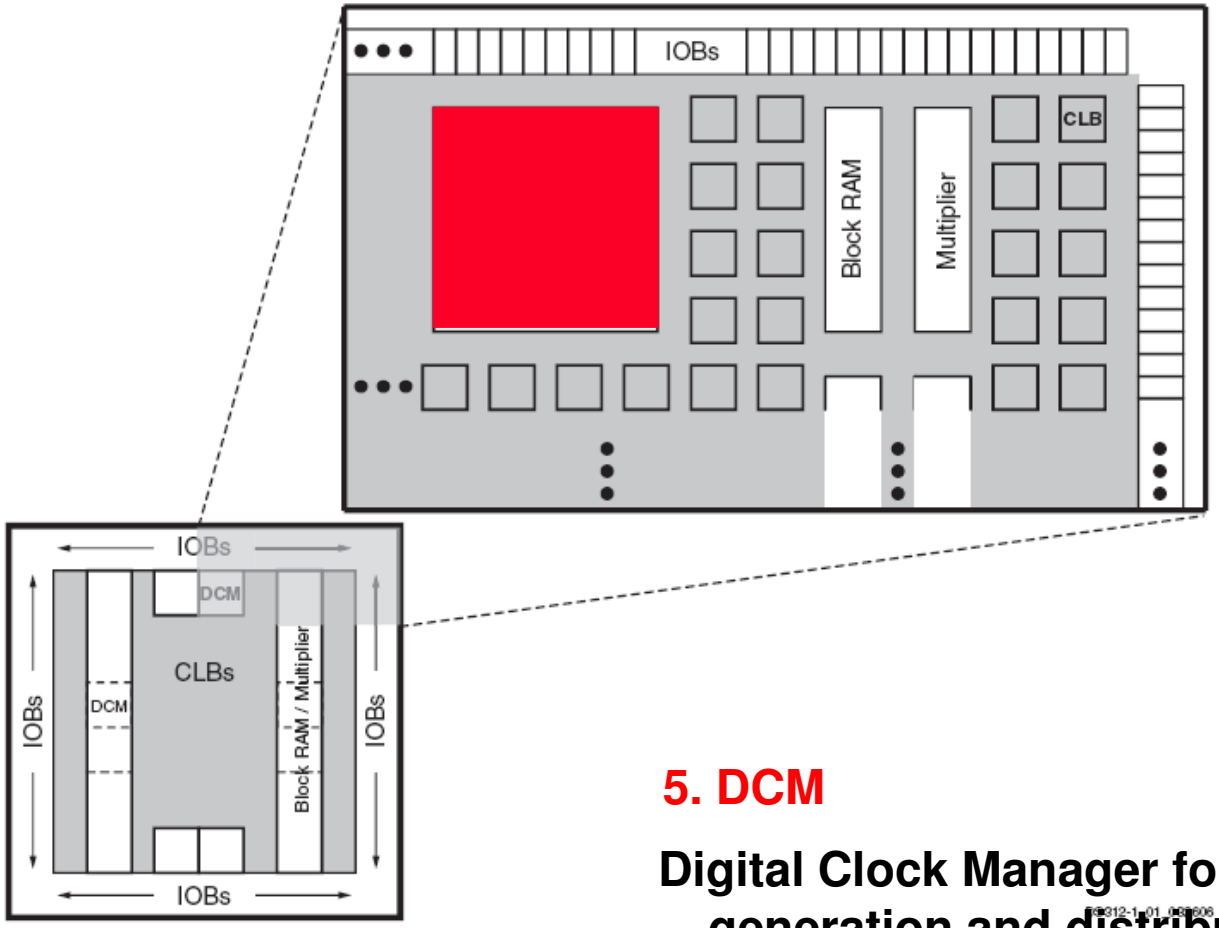
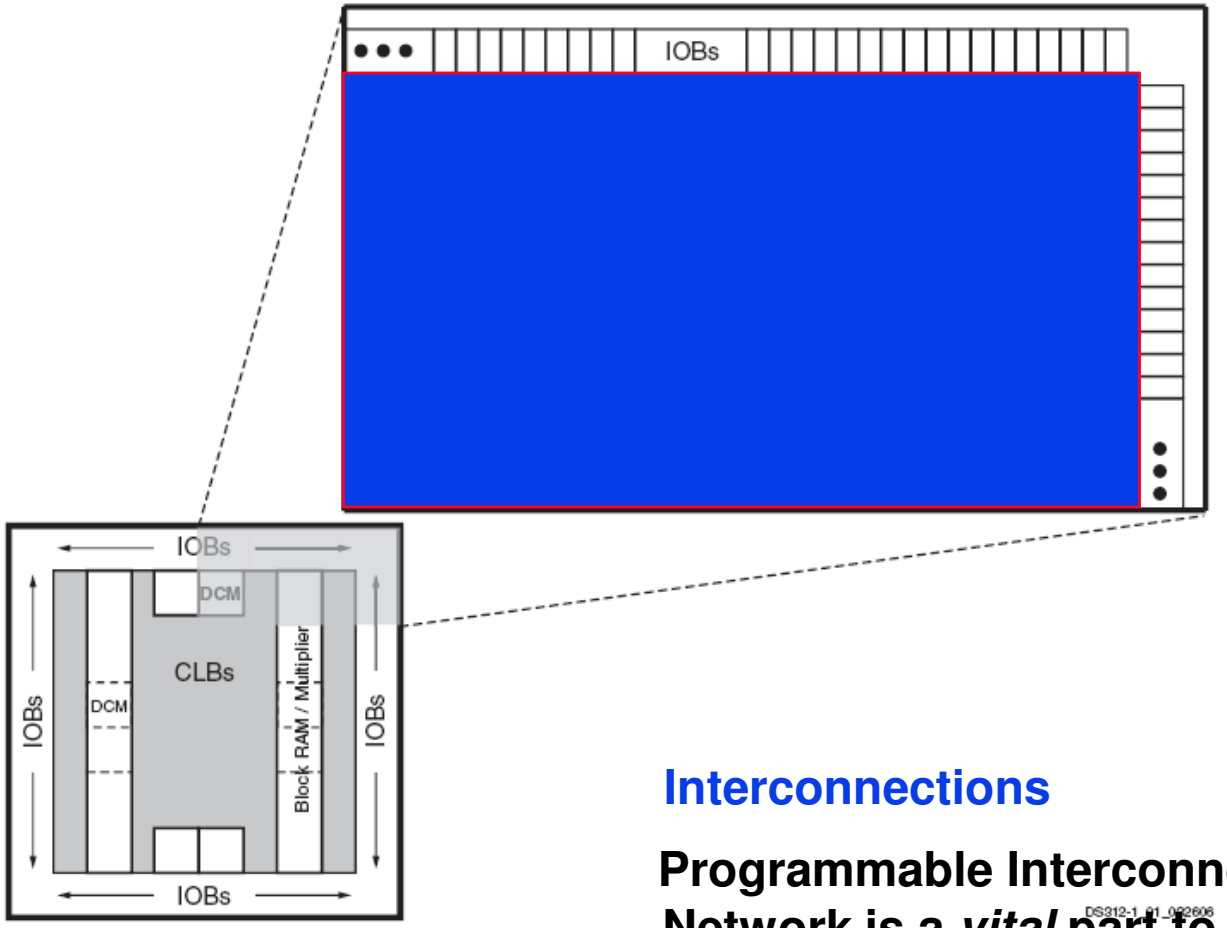


5. DCM

Digital Clock Manager for Clock generation and distribution

Spartan 3

- 5 programmable elements in a regular network



Interconnections

Programmable Interconnection Network is a *vital* part to FPGA

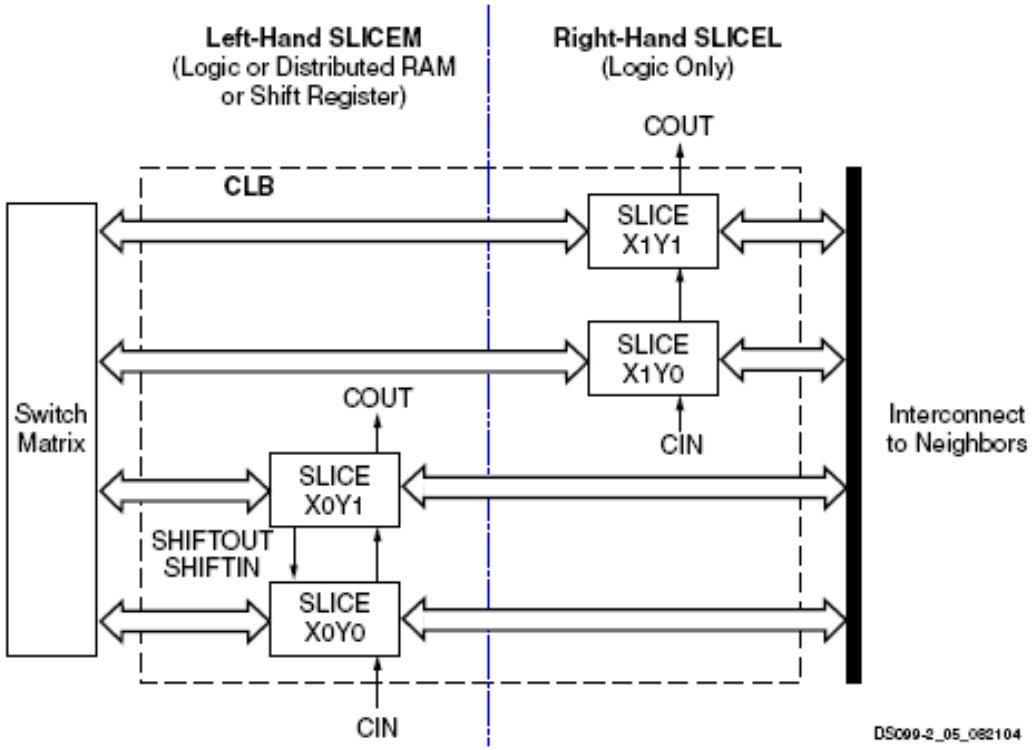
Spartan 3

- In this lecture we discuss two elements
  - CLB
  - Interconnection Network

- Other elements will be discussed later
  - BRAM
  - Multiplier
  - IOB
  - DCM

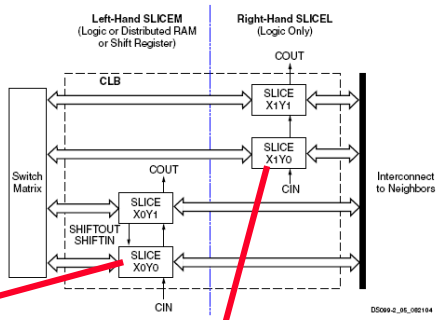
CLB = Configurable Logic Block

- 4 'Slices' per CLB
- Each slice can work as logic (gates + flip-flop), distributed RAM, or shift register
- Switch Matrix connects to FPGA network

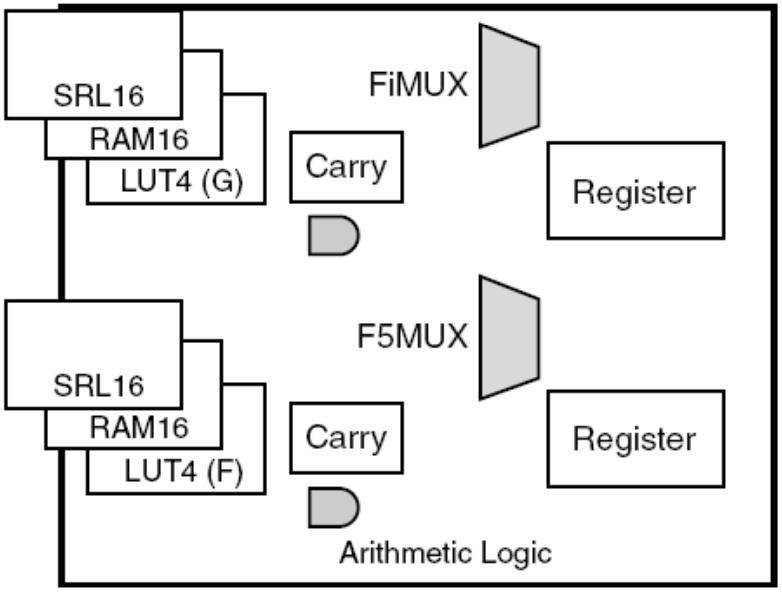


Left-hand and Right-hand slice

- SRL16 = 16-bit shift register (~ 16x1 bit memory)
- RAM16 = 16-bit RAM (~ 16x1 bit memory)
- LUT4 = 4-bit lookup table (~ 4x4bit memory)
- SLICEM = Slice that can work as memory or logic
- SLICEL = Slice that only works as logic

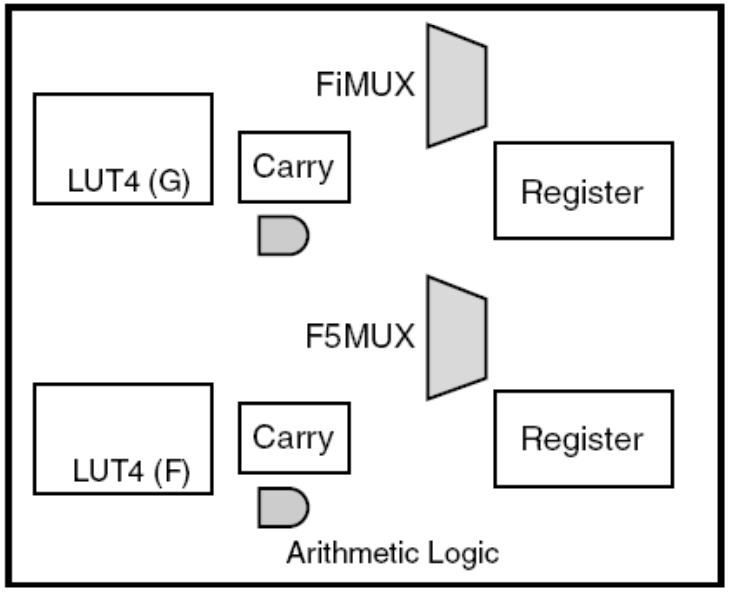


left-hand slice



SLICEM

right-hand slice



SLICEL

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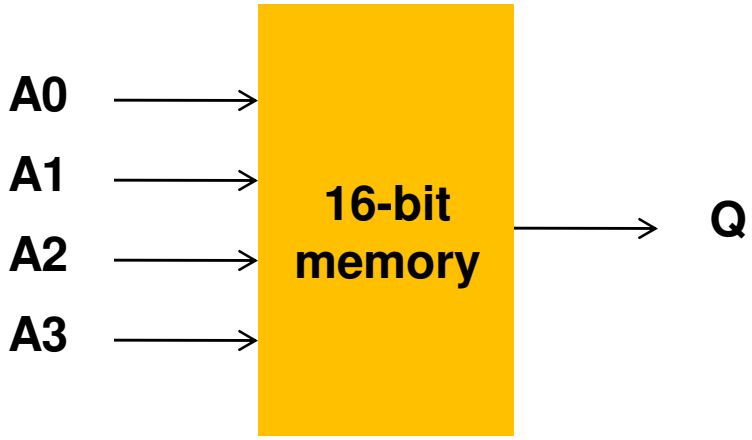
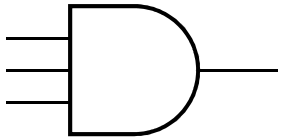
LUT4: basic building block

- RAM memory 4-bit input, 1-bit output
- Can implement any logic function of up to 4 inputs

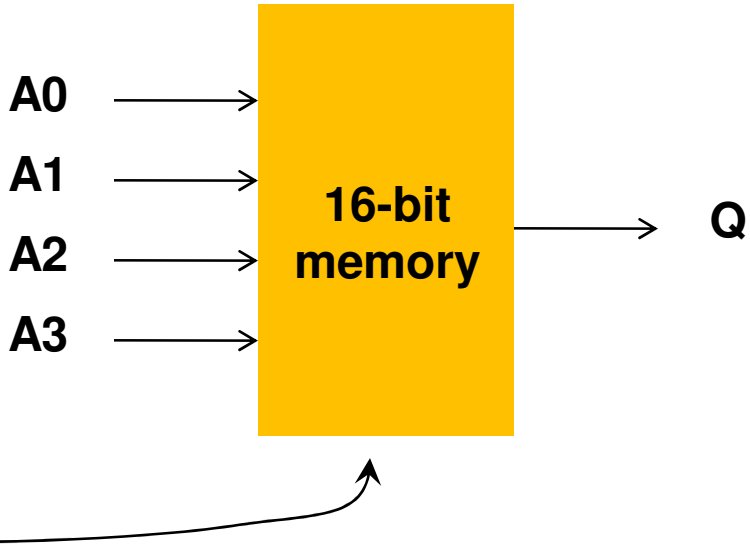


LUT4: basic building block

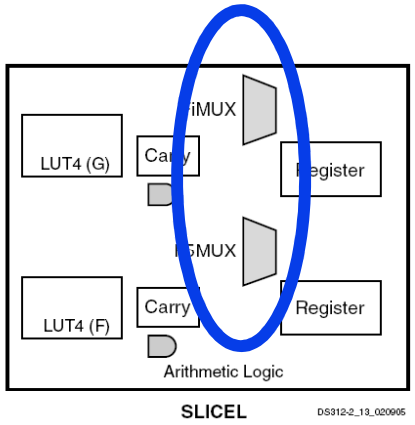
- Example: Implement 3-input AND
- Assume A0 - A2 are used

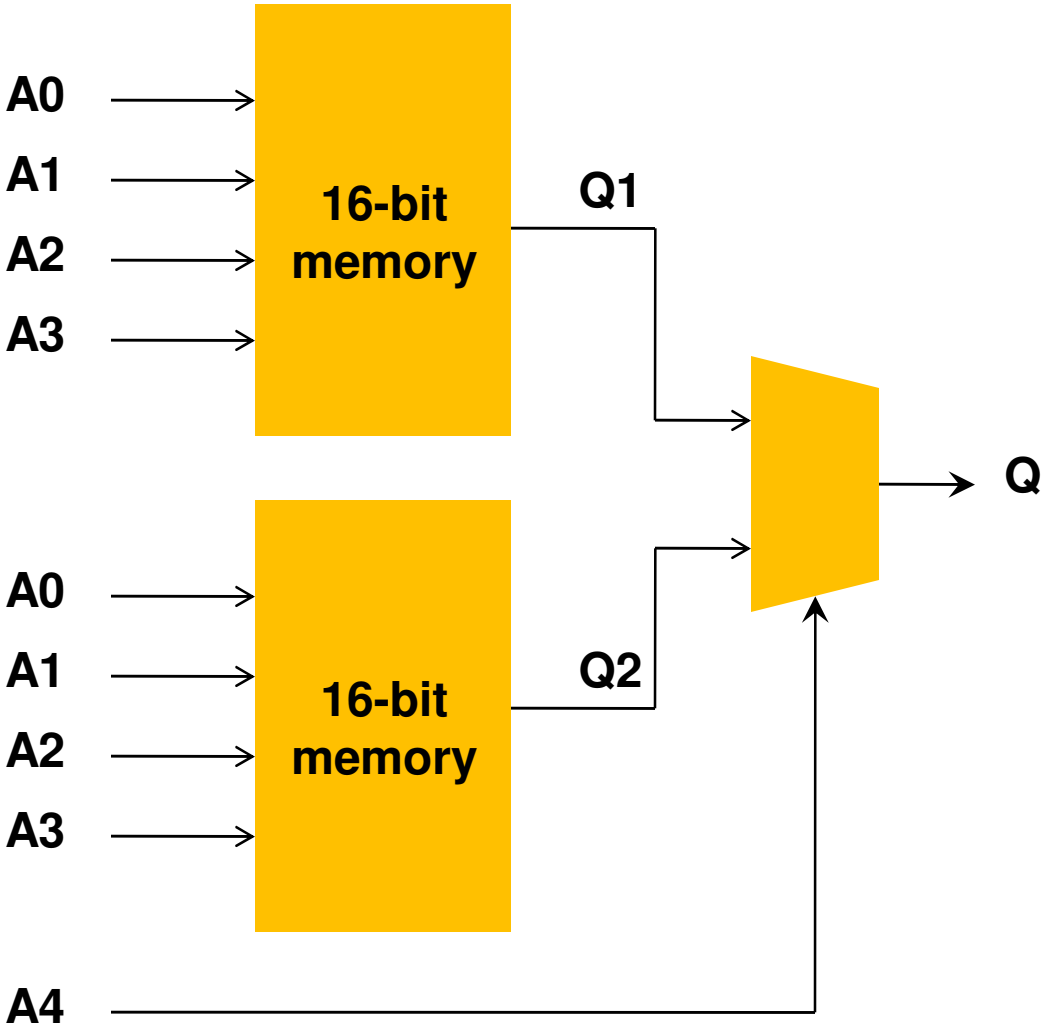


A0	A1	A2	A3	Q
0	0	0	x	0
0	0	1	x	0
0	1	0	x	0
0	1	1	x	0
1	0	0	x	0
1	0	1	x	0
1	1	0	x	0
1	1	1	x	1

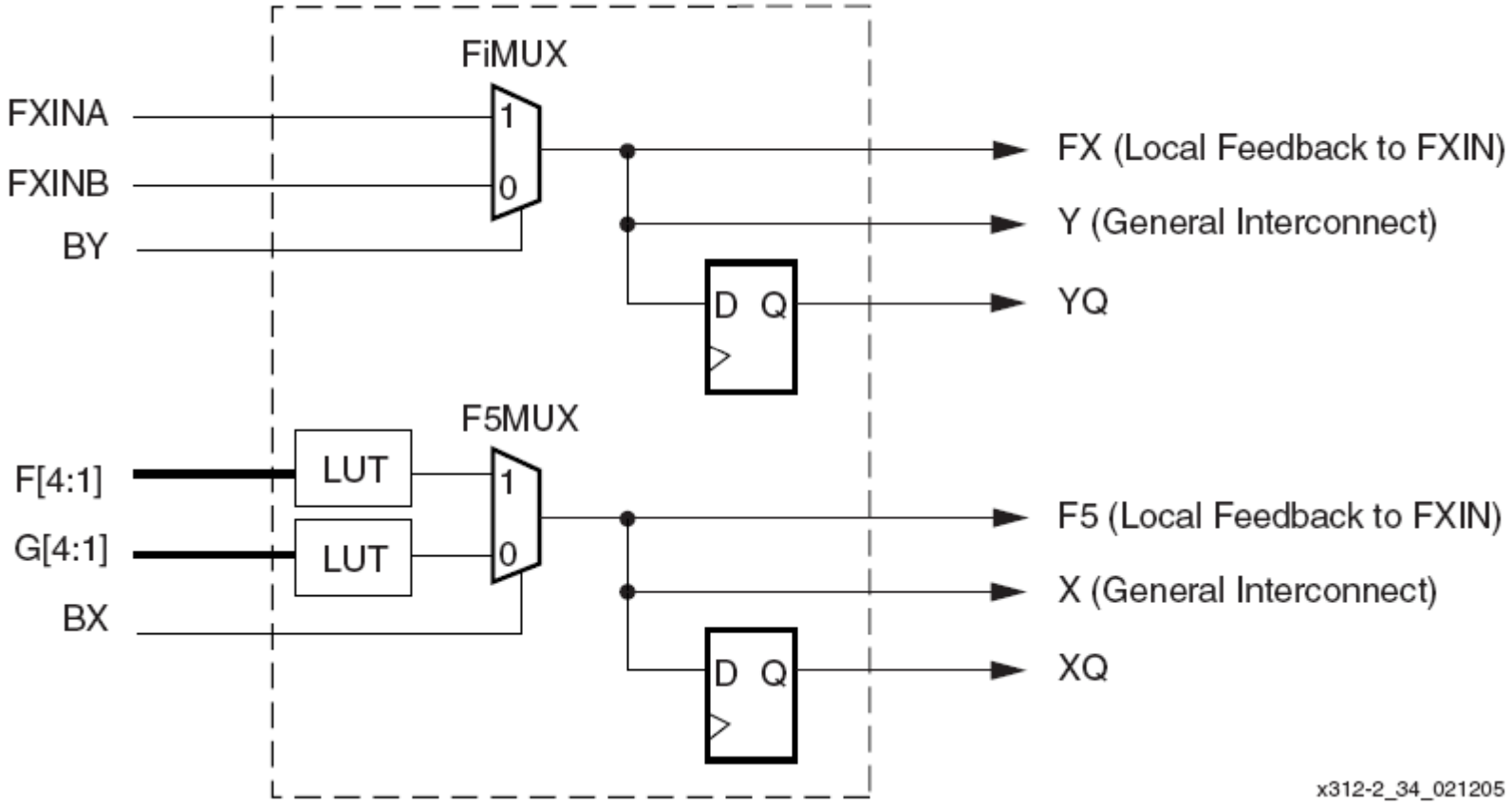


Slice Muxes extend 4-input LUT

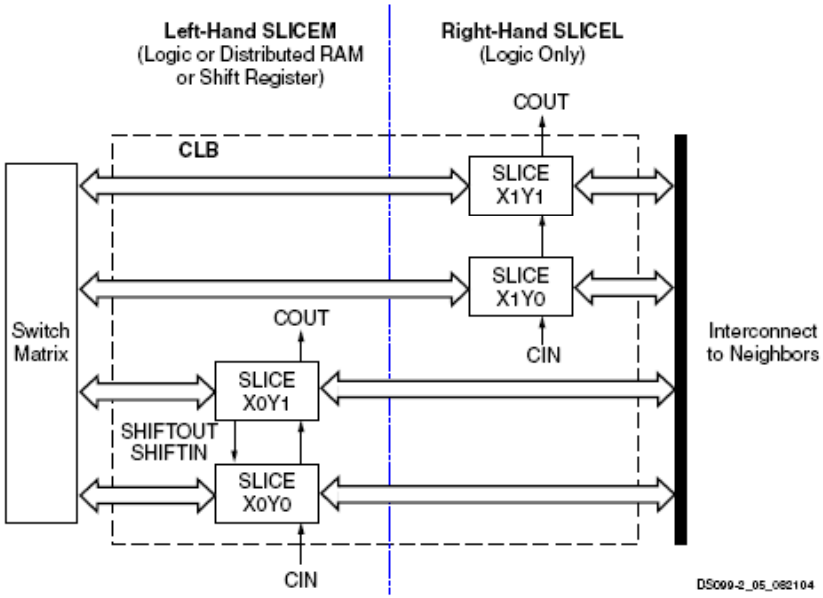


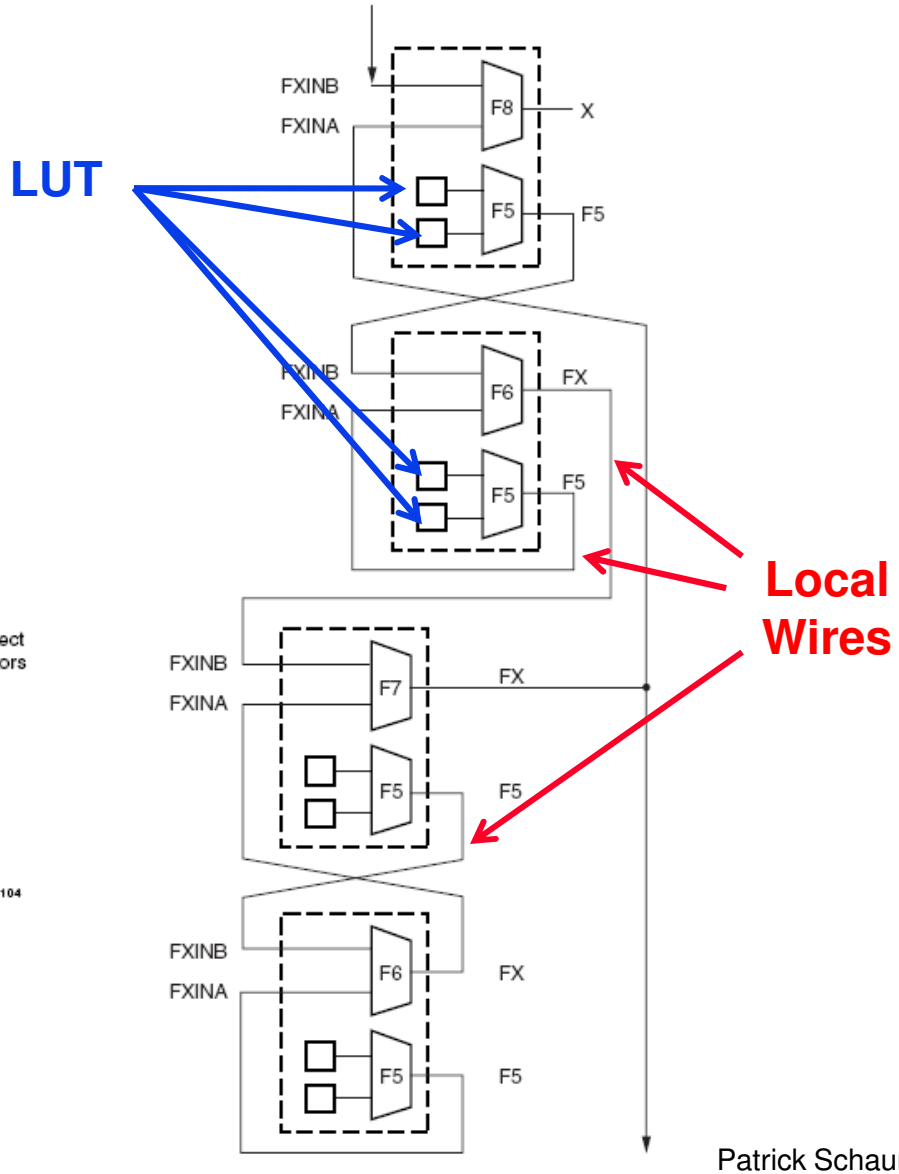


Upper & Lower LUT can be combined further ..

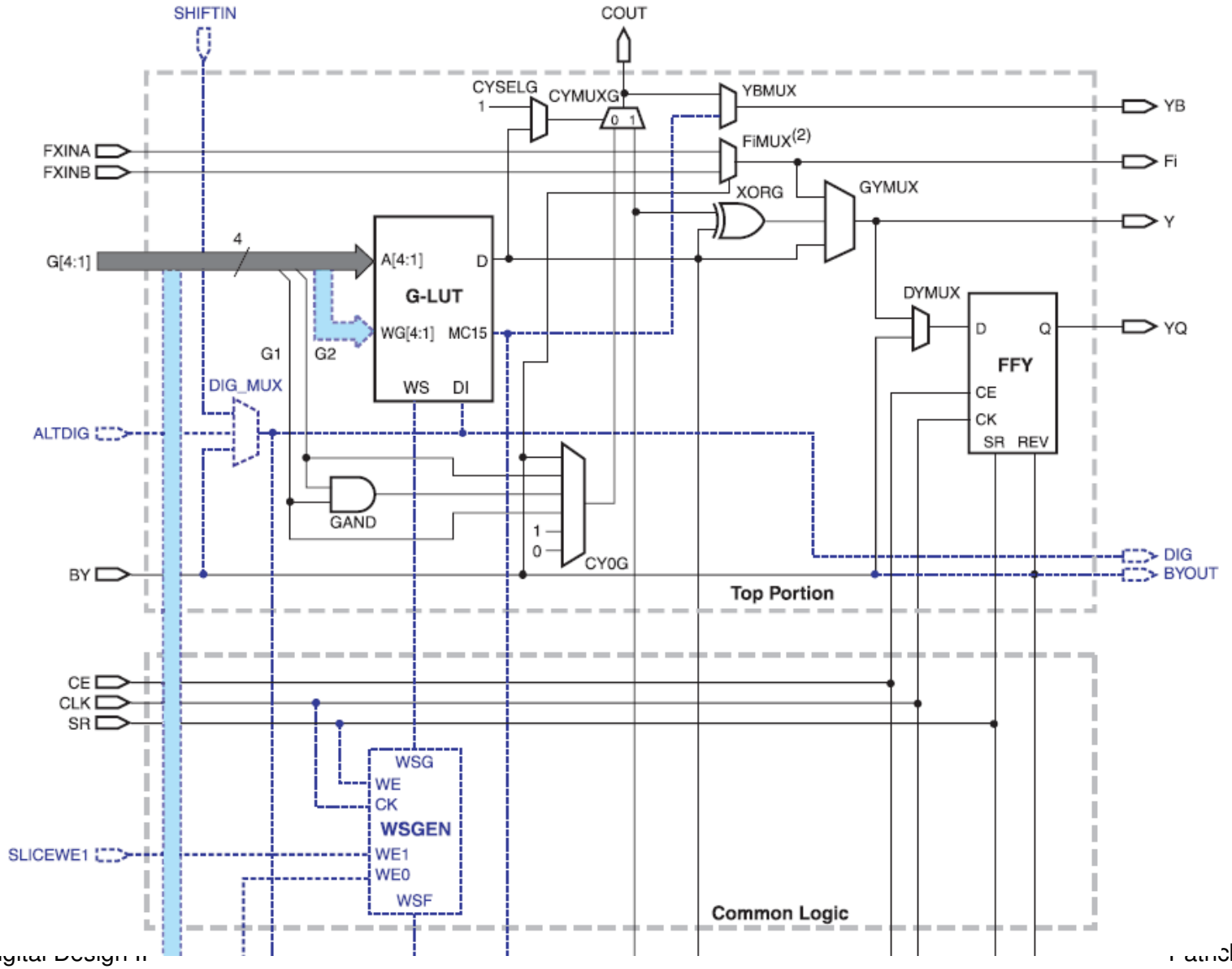


One CLB can implement up to 7-input LUT

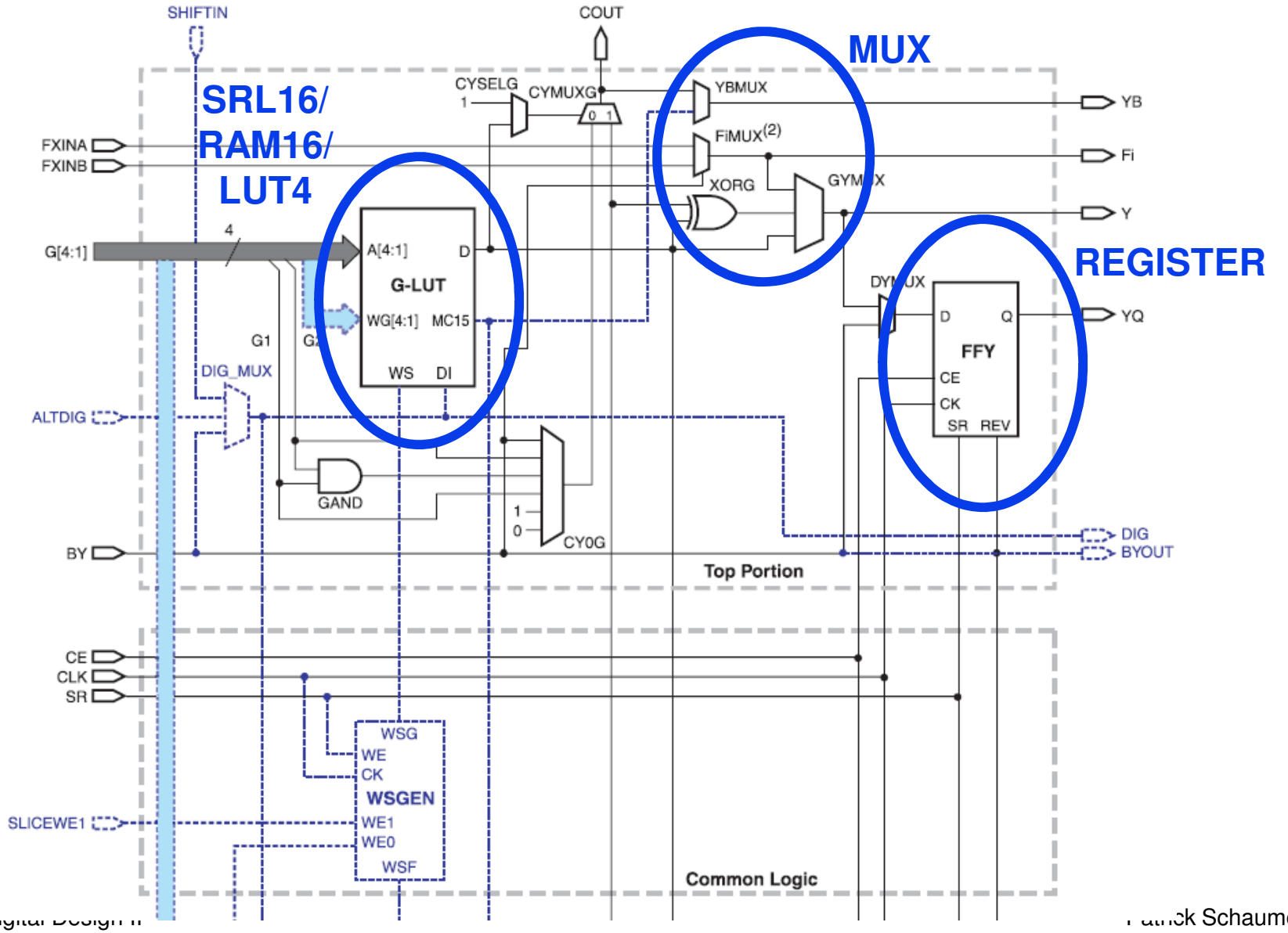




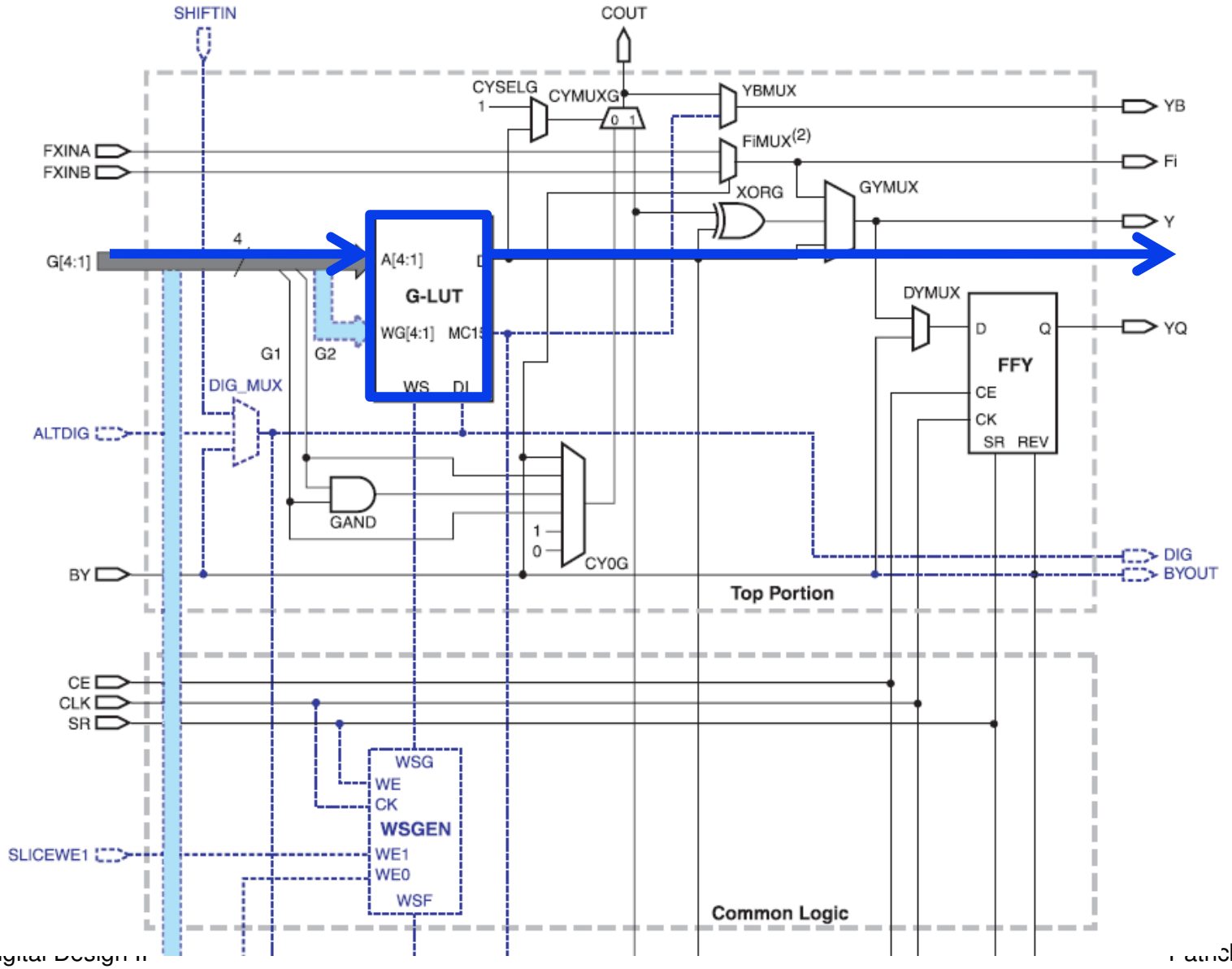
Top half of a (left-hand) slice



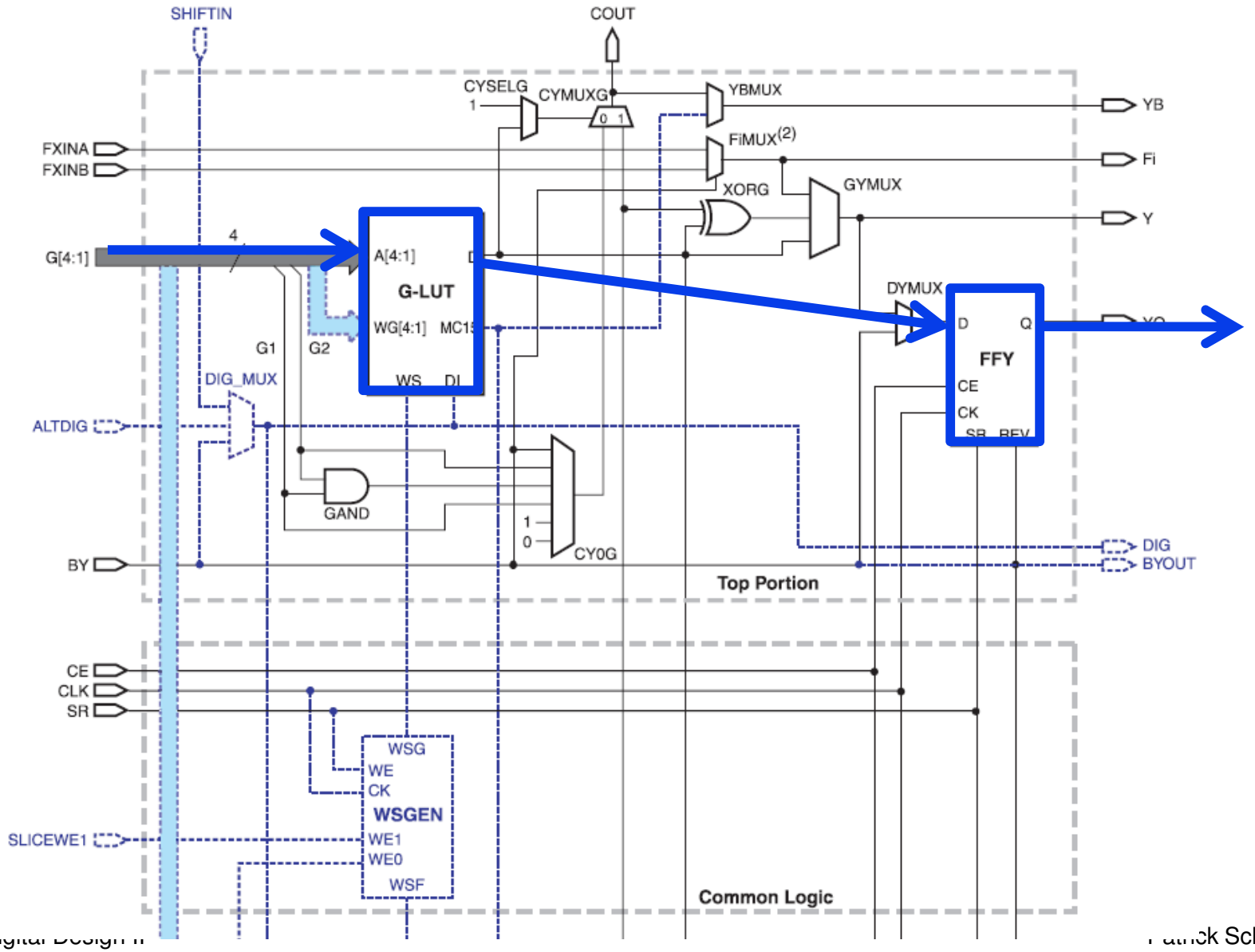
Top half of a (left-hand) slice



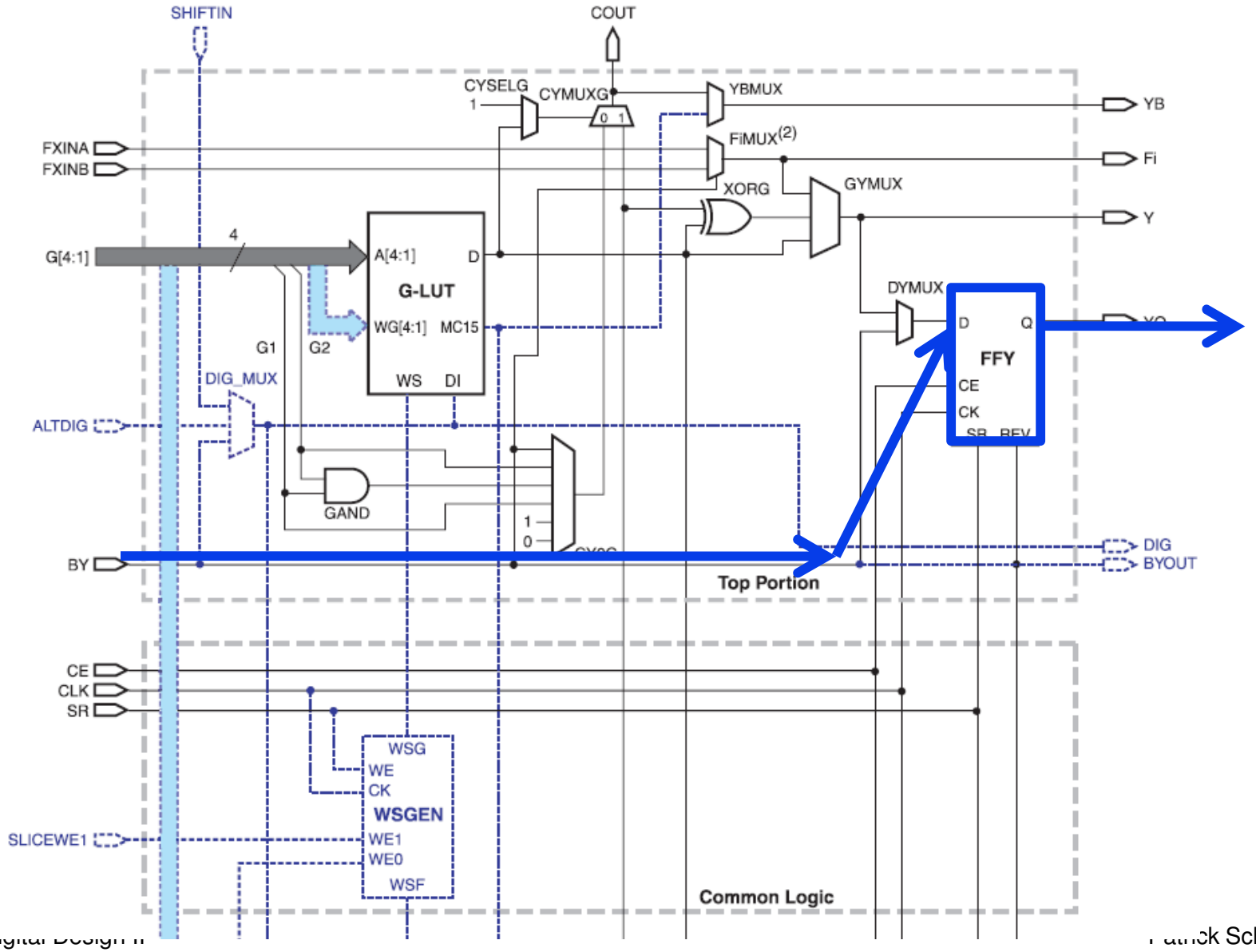
Works only as logic ..



.. or as logic + register

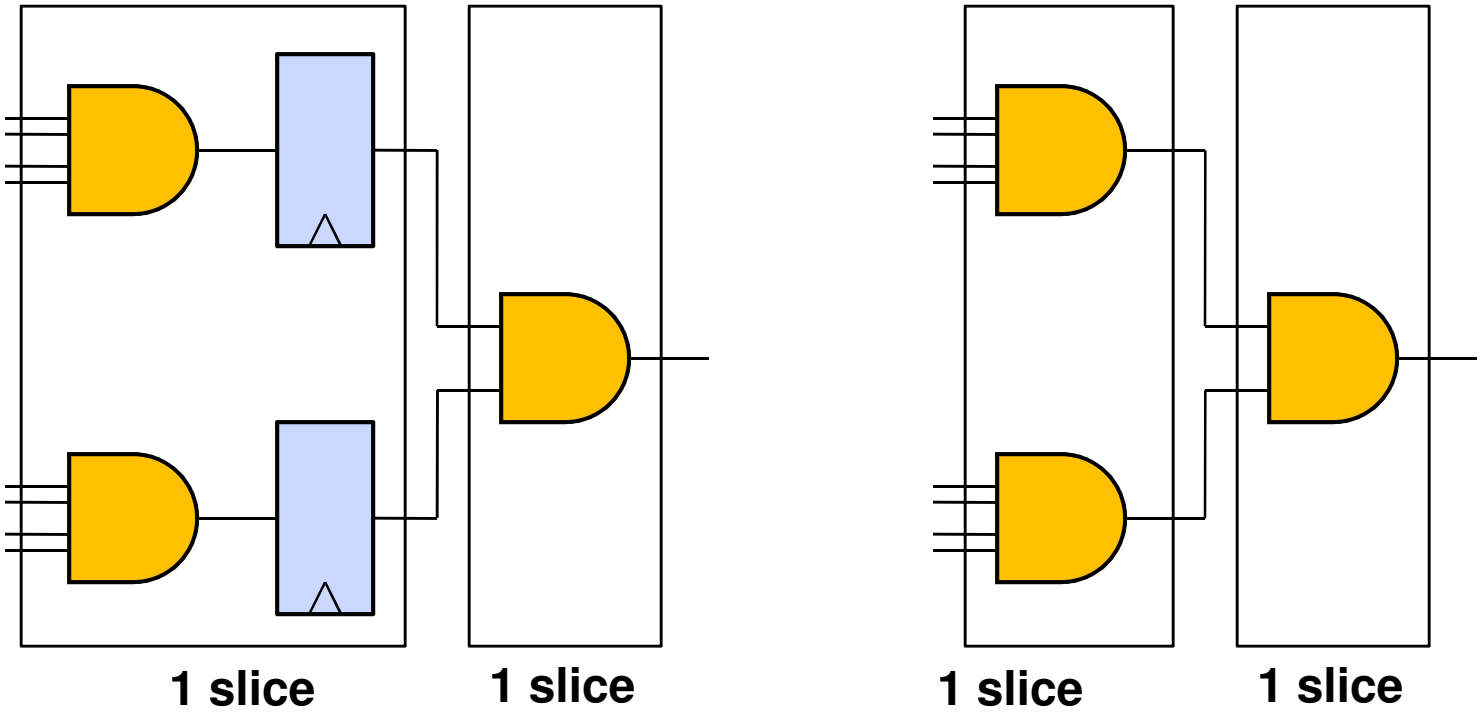


.. or only as register



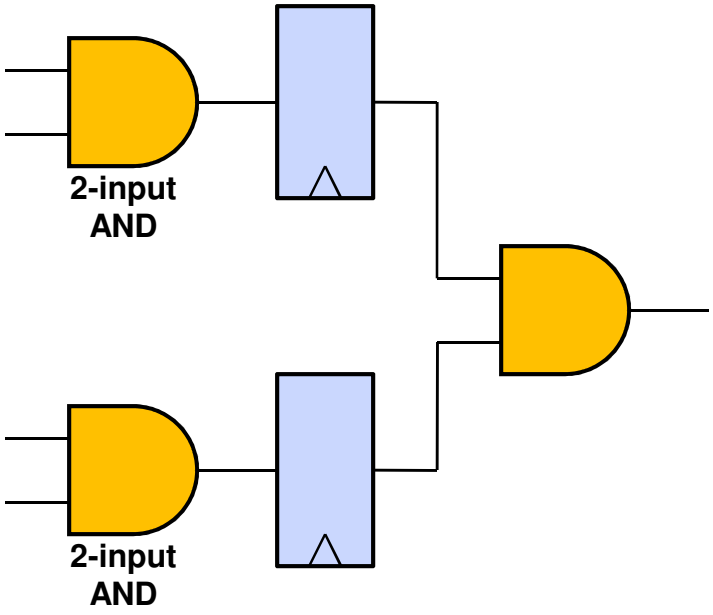
Each LUT comes with a FF, so:

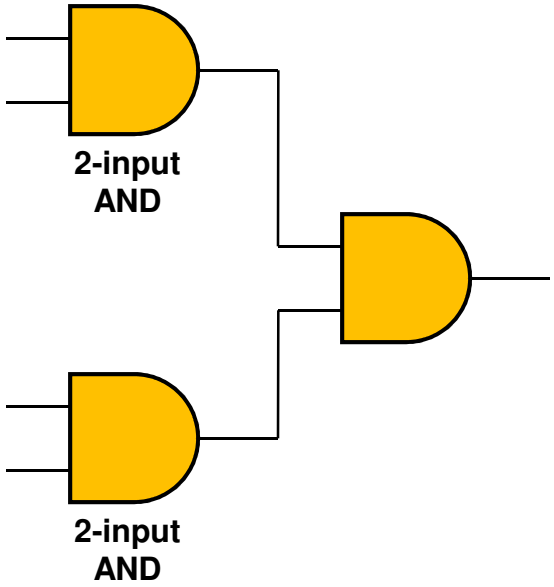
- In an FPGA, the left circuit uses as much slices as the right circuit



What about this case ?

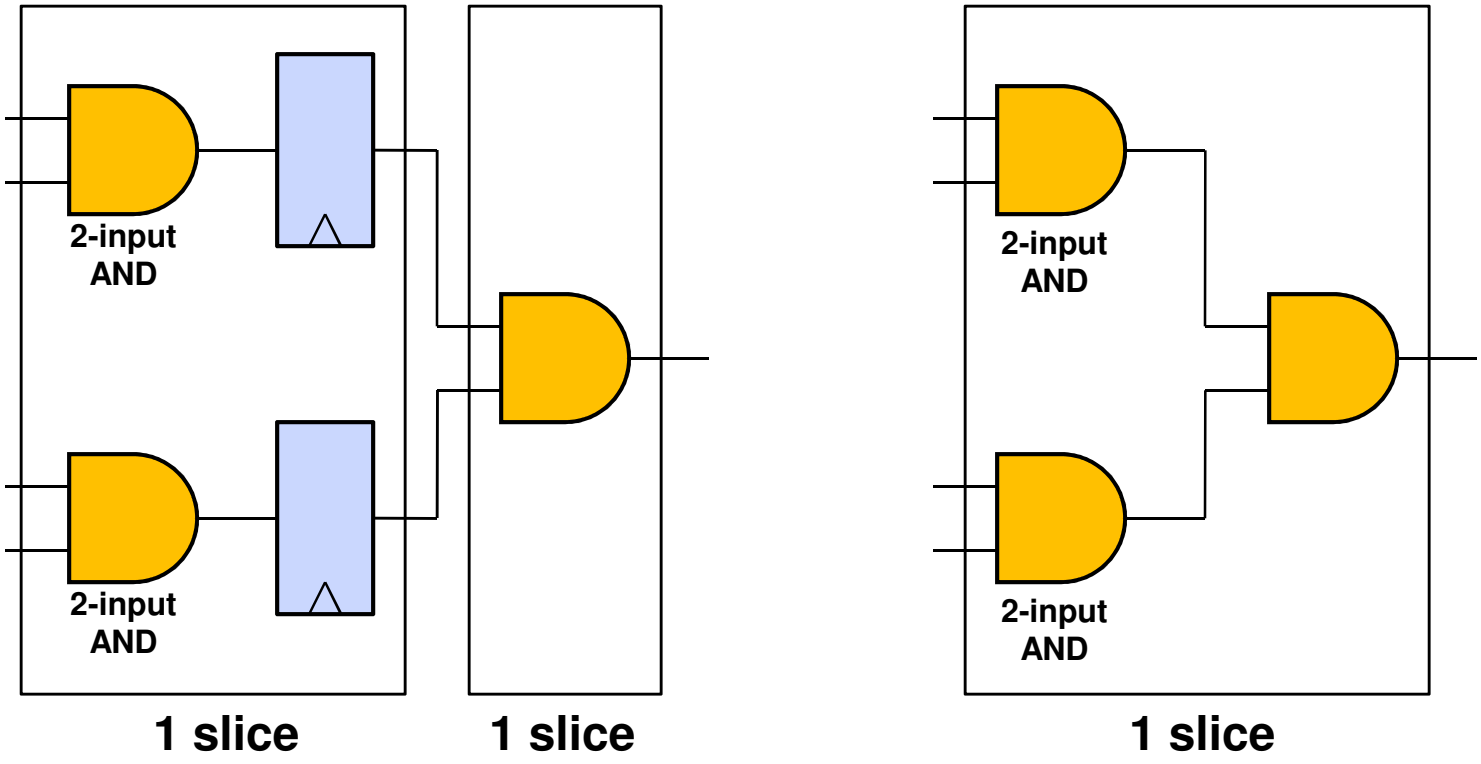
- Do you need the same amount of slices for each circuit?



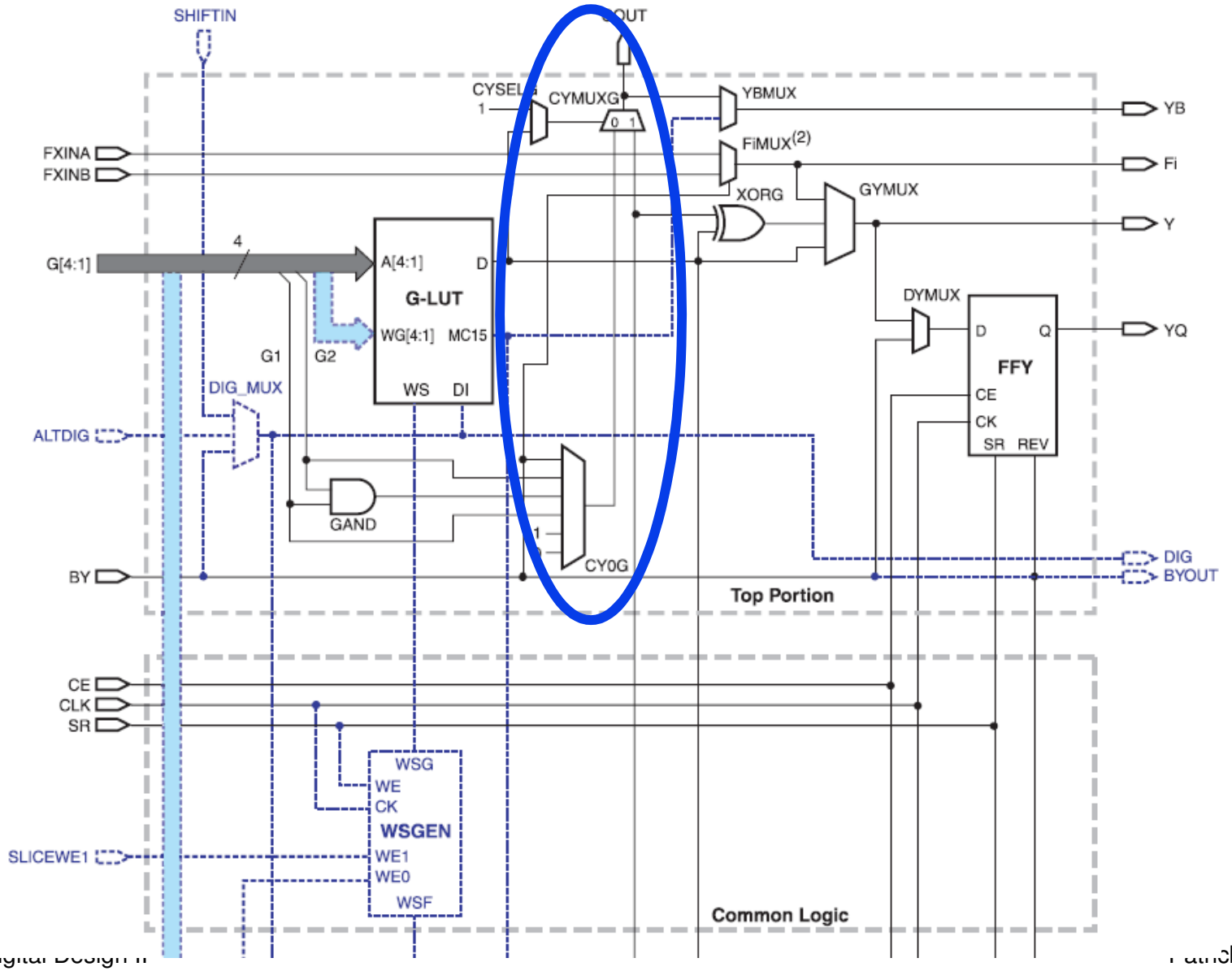


What about this case ?

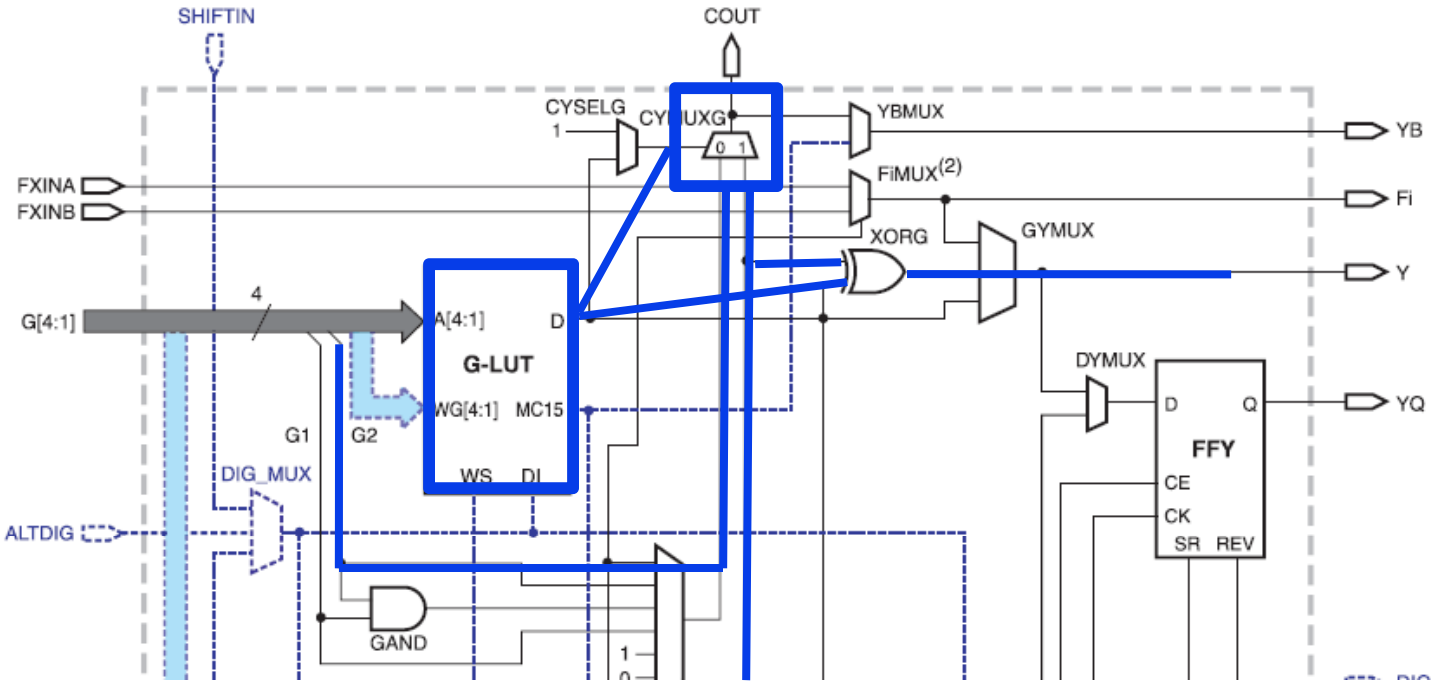
- Do you need the same amount of slices for each circuit?
- No! You can cluster the right circuit in a single slice

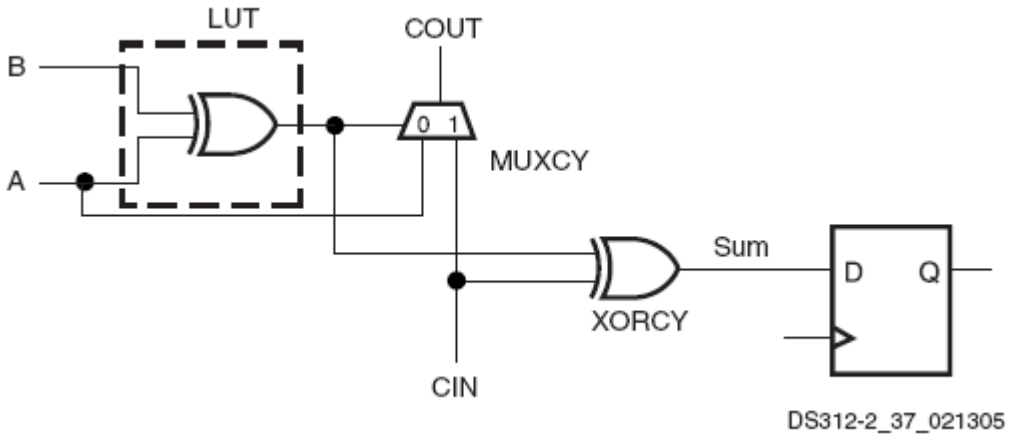


Fast Carry Path (for arithmetic)



Typical use of carry path





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Summary CLB

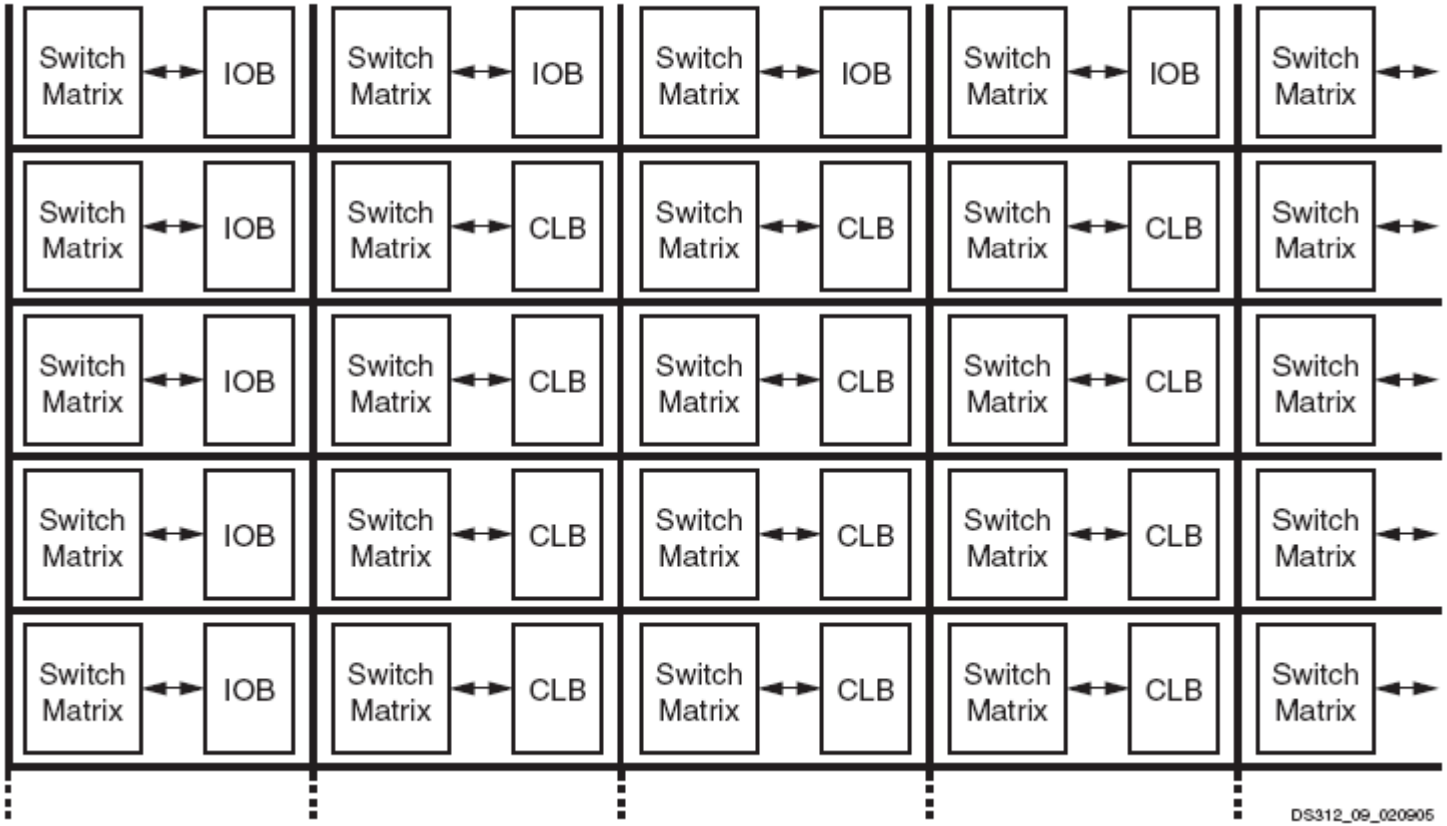
- 1 configurable logic block contains 4 slices
- Each slice contains a combination of
  - 2 LUT
  - 2 flip flop
  - MUXes
  - Carry-logic
- A LUT can operate as
  - Random logic function of 4 inputs
  - 16-bit RAM
  - 16-bit shift register
- Tools report area results in slices
  - Slices can be many different things, depending on configuration

Interconnect Network

- Interconnections are THE critical component in an FPGA
  - Largest physical area on a die
  - Largest power consumption
  - In most cases, wire delay becomes performance bottleneck
- Ironically, interconnections are hardly mentioned as a feature in FPGA product literature
  - Engineers like to hear about the number of CLBs in an FPGA, not about the number of wires between CLBs ...
- FPGA interconnect network is a hierarchical architecture
  - Many fast, short wires with small drive capacity
  - Few longer wires with high drive capacity
  - Like a slice architecture, design of interconnect network is a 'secret sauce' of the FPGA..

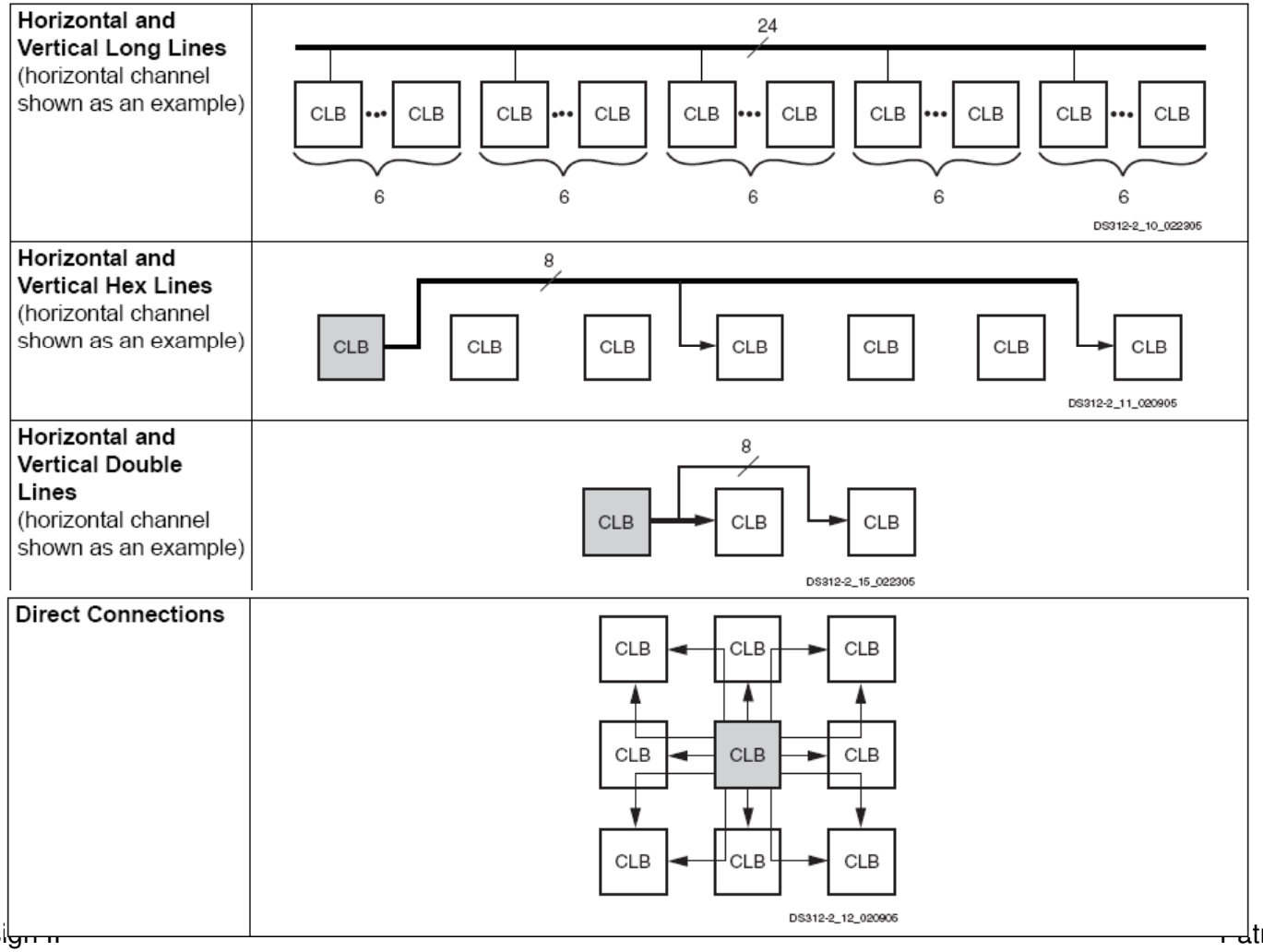
Interconnection Network in Spartan 3

- CLBs connect to 'switch matrix' which connects to the on-chip network
- Each switch matrix interconnects many different wires



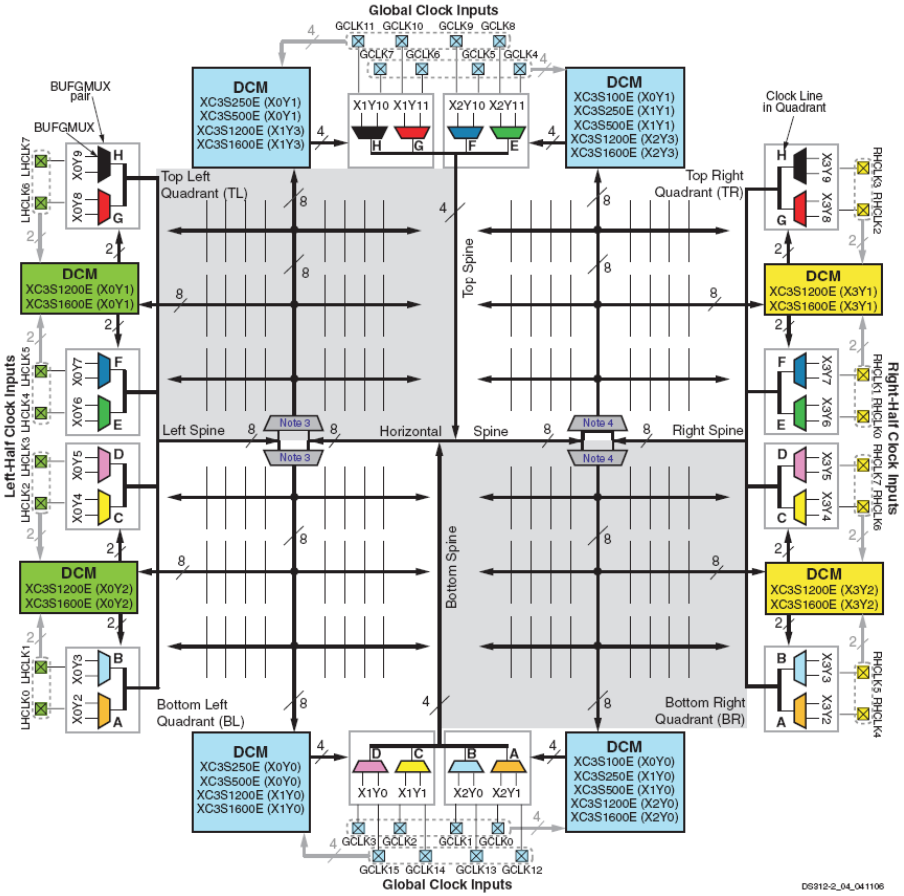
Interconnection Network

- 4 wire types connected to switch matrix



Interconnection Network

- Clock signals are distributed with a separate, dedicated network
  - Another reason to avoid gated clocks ..
- A recursive 'fish-bone' network ensures that clock arrives everywhere at the same time
- Clock signals generated externally or else inside of 'DCM'
  - DCM can create multiply/ divide external clock to a different on-chip clock



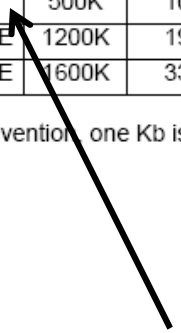
Now, we understand databook figures

Table 1: **Summary of Spartan-3E FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.



The Spartan 3E starter kit has a 3ES500 FPGA

Summary on 3ES500

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Notes:

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XC3S500E = 500K 'system gates'

10,476 Logic Cells

A 'Logic Cell' is the unit of configuration in an FPGA.
It consists of a lookup table and a flip-flop.
In the case of Xilinx, 1 LC = 2.25 LUT ..

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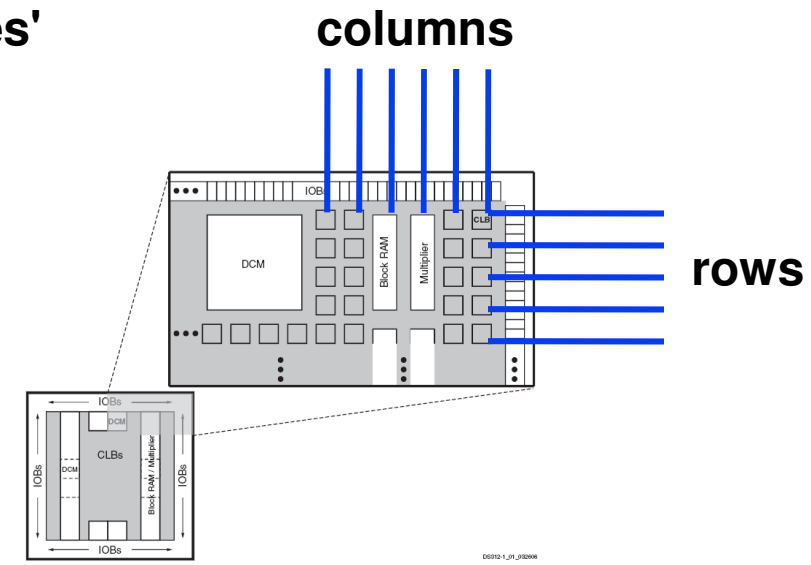
46 rows, 34 columns



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Notes:

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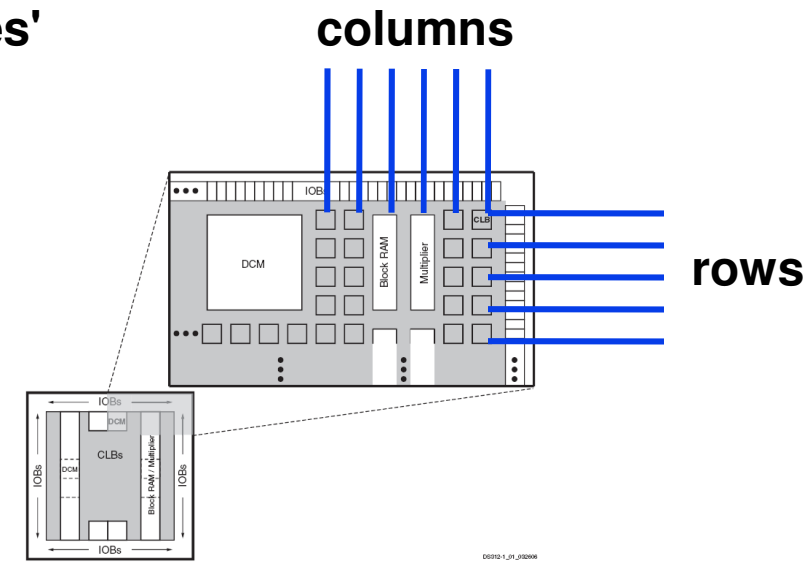
46 rows, 34 columns

46 x 34 = 1564 positions

1,164 CLB's

So 400 'positions' used for other things (RAM, ...)



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XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

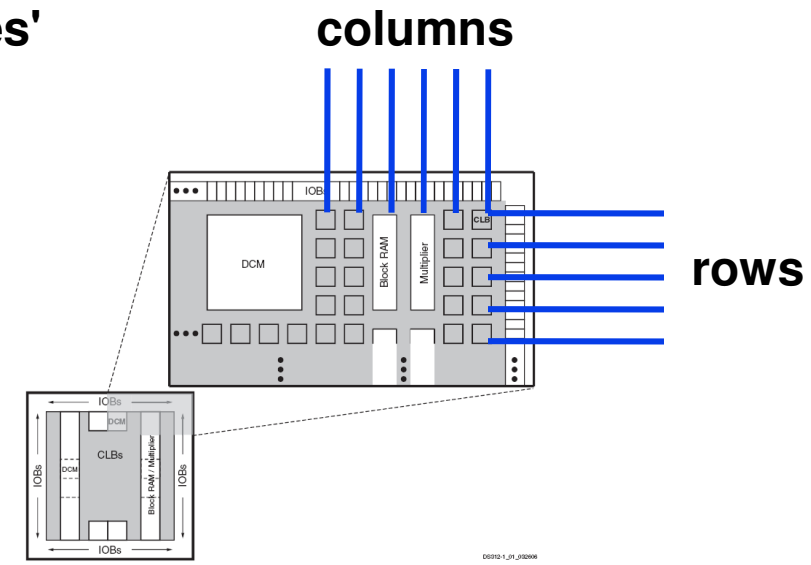
XC3S500E = 500K 'system gates'

1,164 CLB's

4,656 Slices

Each CLB contains 4 'Slices'

A Slice contains 2.25 LC's
2.25 x 4,656 = 10,476



Summary on 3ES500

Table 1: **Summary of Spartan-3E FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
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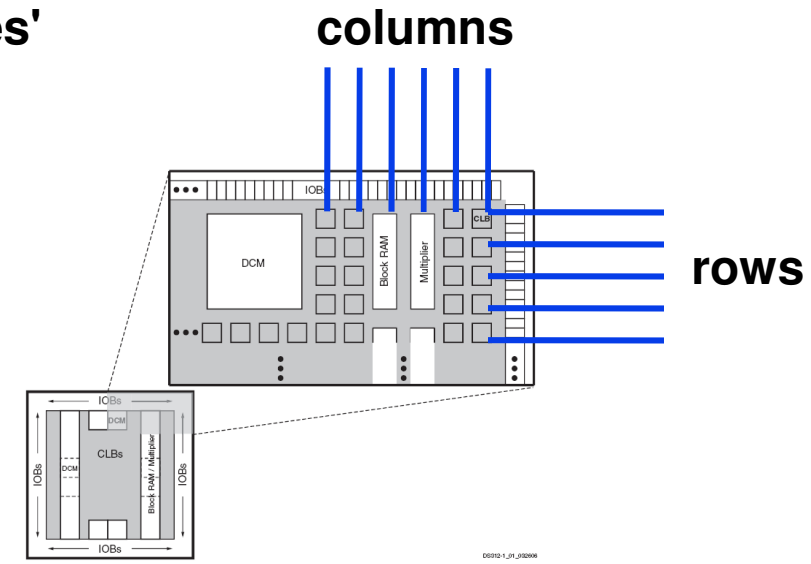
1,164 CLB's

4,656 Slices

73K 'Distributed RAM' Bits

Each Slice contains
4 x 4 bits = 16 bits of 'RAM'
4,656 x 16 = 74496 = 72.75K



Summary on 3ES500

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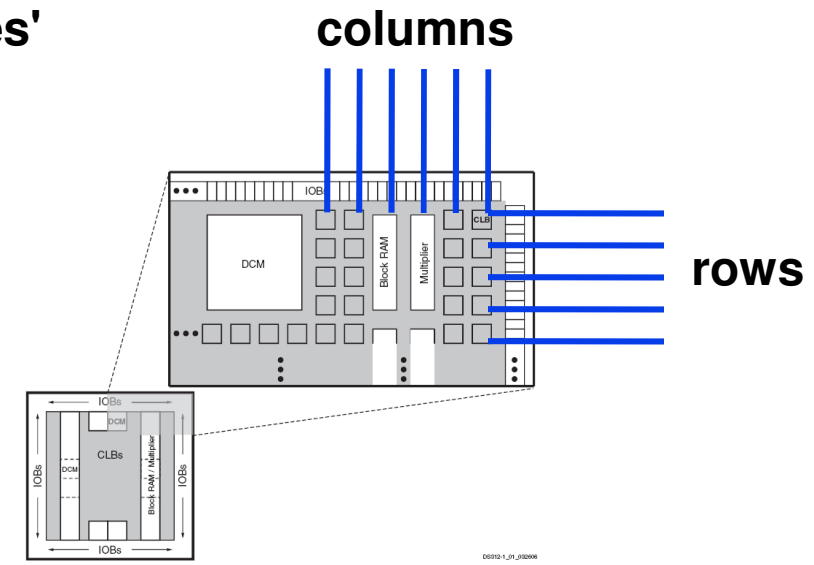
1,164 CLB's

4,656 Slices

360K of Block RAM bits
18 Kbit per Block RAM

Thus 360/18 = 20 Block RAM



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Notes:

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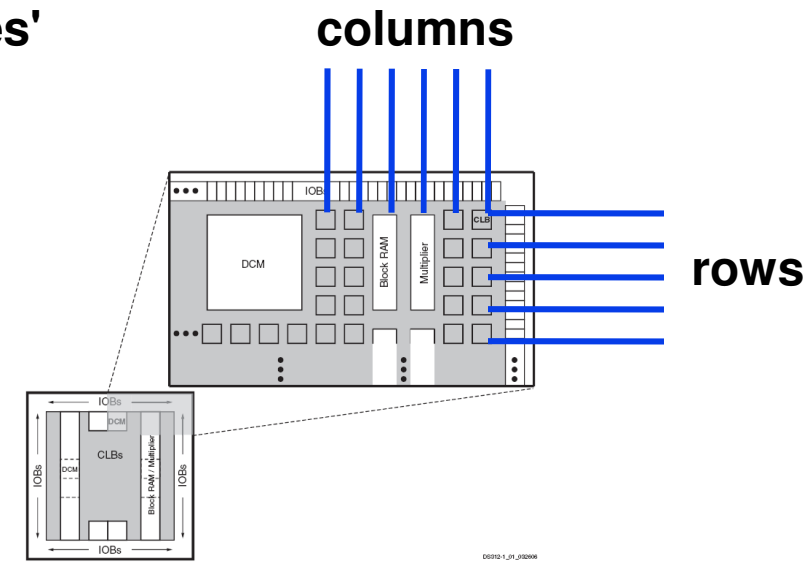
XC3S500E = 500K 'system gates'

1,164 CLB's

4,656 Slices

360K of Block RAM bits
20 Multipliers

Next to each Block RAM there is a multiplier cell



Now, we also understand tool output

The SHA-1 Design, revisited

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	503	9,312	5%	
Number of 4 input LUTs	1,676	9,312	17%	
Logic Distribution				
Number of occupied Slices	995	4,656	21%	
Number of Slices containing only related logic	995	995	100%	
Number of Slices containing unrelated logic	0	995	0%	
Total Number of 4 input LUTs	1,836	9,312	19%	
Number used as logic	1,676			
Number used as a route-thru	32			
Number used as Shift registers	128			
Number of bonded IOBs	196	232	84%	
Number of GCLKs	1	24	4%	
Total equivalent gate count for design	24,308			
Additional JTAG gate count for IOBs	9,408			

Now, we also understand tool output

The SHA-1 Design, revisited

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Total equivalent gate count for design	24,308			
Additional JTAG gate count for IOBs	9,408			

Used 995 Slices (2x995 = 1990 LUT's at most)
Used 1836 LUTs of 1990 possible LUTs
Used 1676 of 1836 occupied LUTs for actual logic
Used 503 Flip Flops of (2x995 = 1990 Flip Flops at most)

Summary FPGA

- FPGA contains 5 elements + interconnection network
  - CLB
  - RAM
  - Multiplier
  - DCM
  - IOB
- A 'gate-level netlist' is mapped on an FPGA by configuring these elements
  - Choose CLB configuration (LUT, flip-flop, carry logic, ..)
  - Choose interconnections in network